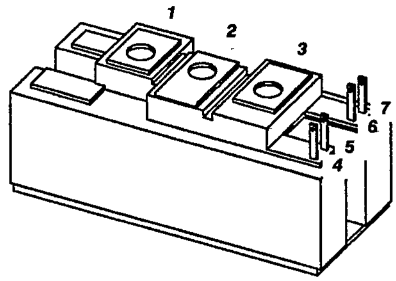
Siliconix incorporated

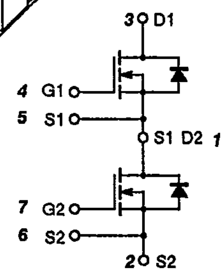
SPMB50A500

Power MOSFET Module



PRODUCT SUMMARY

$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)	V_{ISOL} (V)
500	0.100	50	2500



FEATURES:

- Half-bridge Circuit
- Fast Intrinsic Diode (270 ns)
- Short Circuit Withstand Time Rated
- Isolated Plastic Package
- Very Low On-Resistance
- High Frequency Operation (>20 kHz)

APPLICATIONS:

- Uninterruptible Power Supply
- Switch-mode Power
- Motor Control
- Arc Welding Inverters
- Induction Heating

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	±20	
Operating Drain Current[1]	I_D	50	A
Pulsed Drain Current[2]	I_{DM}	200	
Total Power Dissipation (per Transistor)	P_D	300	W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	-40 to 125	
Isolation Voltage (RMS)	V_{ISO}	2500	V
Short Circuit Withstand Time (V_{DD} = 350 V, V_{GS} = 10 V)	SCWT	12	μS

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MECHANICAL DATA

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Mounting Torque (Maximum)	Mounting Base (M6)		50 (43 in-lbs)	kgf.cm
	Terminals (M5)		50 (43 in-lbs)	
Mass			220	g
Thermal Resistance (Junction to Baseplate per MOSFET)		R_{thJC}	0.41	°C/W

[1]For duty cycles ≤ 60%.
[2]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 10).

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)				LIMITS		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP	MIN	MAX	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		500		V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 10 mA		1.5	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V			1.0	mA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125°C			4.0	
Drain-Source On-State Resistance[1]	$r_{DS(ON)}$	V_{GS} = 15 V, I_D = 25 A	0.08		0.10	Ω
		V_{GS} = 15 V, I_D = 25 A, T_J = 125°C	0.15		0.22	
Forward Transconductance[1]	g_{fs}	V_{DS} = 10 V, I_D = 25 A	20			S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	11000			pF
Output Capacitance	C_{oss}		1600			
Reverse Transfer Capacitance	C_{rss}		800			
Total Gate Charge[2]	Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 15 V, I_D = 50 A	400		600	nC
Gate-Source Charge[2]	Q_{gs}		40		64	
Gate-Drain Charge[2]	Q_{gd}		160		320	
Turn-On Delay Time[2]	$t_{d(on)}$	V_{GS} = 15 V, R_L = 12 Ω I_D ≃ 25 A, V_{DD} = 300 V, R_G = 10 Ω	70			ns
Rise Time[2]	t_r		100			
Turn-Off Delay Time[2]	$t_{d(off)}$		950			
Fall Time[2]	t_f		250			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				50	A
Pulsed Current[3]	I_{SM}				200	
Source-Drain Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0 V			1.5	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, dI_F/dt = 200 A/µs, I_F = 25 A V_R = 100 V	270		300	ns

Siliconix modules utilize the intrinsic Drain-Source diodes of the MOSPOWER chips as anti-parallel diodes. Through proprietary technology these diodes are processed for fast recovery and low V_{SD}. This means that the current handling capability of Siliconix modules is symmetrical, that is, the diode portion can handle the same peak and average current as the transistor and has the same low thermal impedance.

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 10).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

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Figure 1. Output Characteristics

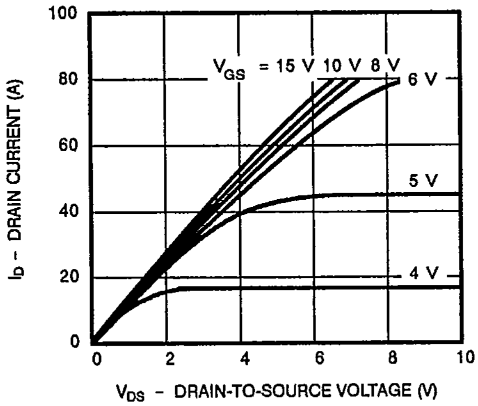


Figure 2. Transfer Characteristics

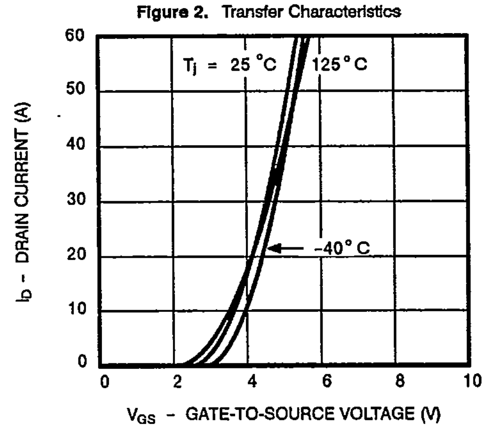


Figure 3. Transconductance

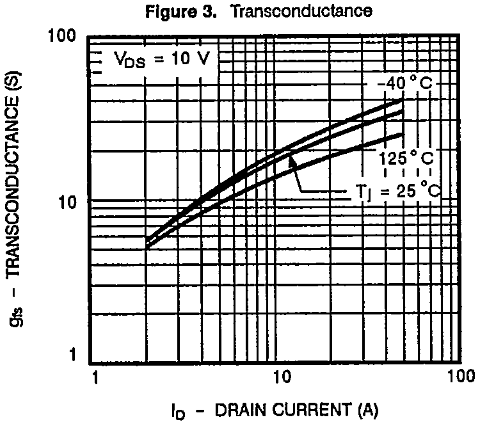


Figure 4. On-Resistance

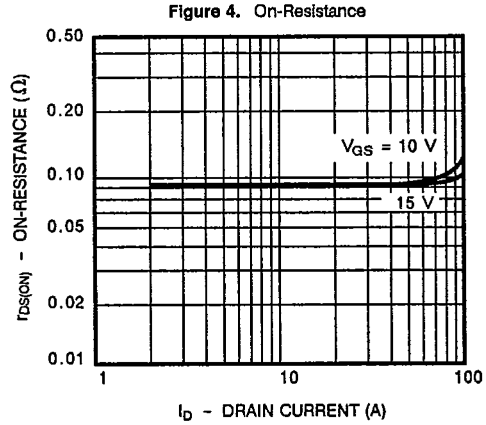


Figure 5. Capacitance

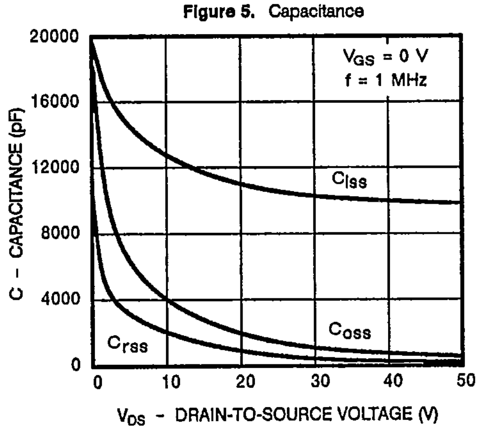
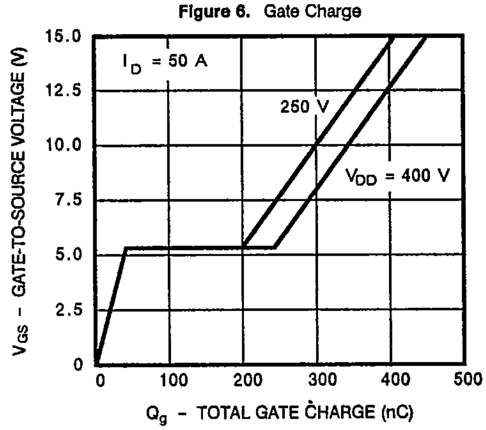


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

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Figure 7. On-Resistance vs.Junction Temperature

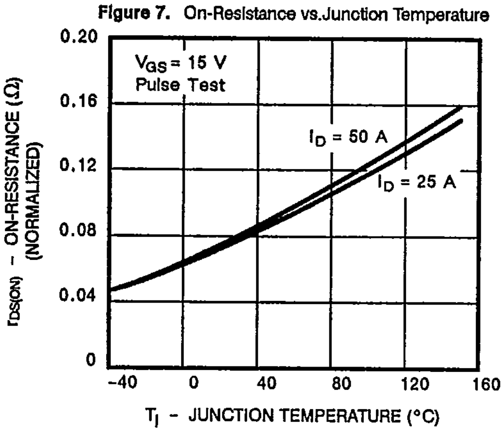
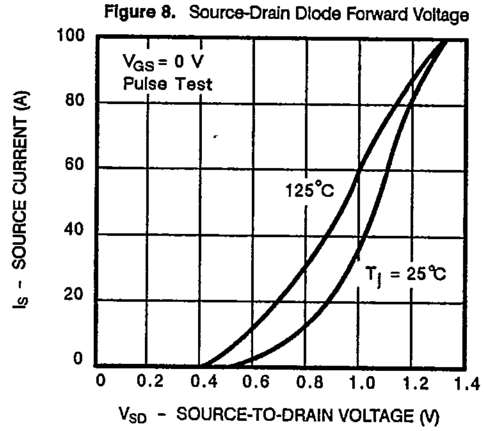
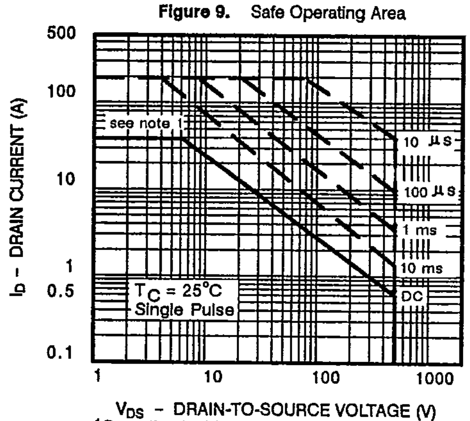


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 10. Normalized Effective Transient Thermal Impedance, Junction-to-Case