MDA970A1
thru
MDA970A6

MOTOROLA

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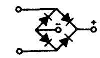
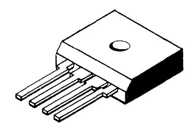
Designers Data Sheet



SINGLE-PHASE FULL-WAVE BRIDGE

4 AMPERES
50-600 VOLTS



INTEGRAL DIODE ASSEMBLIES

. . . diffused silicon dice interconnected and transfer molded into rectifier circuit assemblies for use in application where high output current/size ratio is of prime importance. These devices feature:

- Void-free, Transfer-molded Encapsulation to Assure High Resistance to Schock, Vibration, and Temperature Extremes
- High Dielectric Strength
- Simple, Compact Structure for Trouble-free Performance
- High Surge Capability — 100 Amps

Designers Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	MDA970A1	MDA970A2	MDA970A3	MDA970A5	MDA970A6	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	50	100	200	400	600	Volts
RMS Reverse Voltage	$V_{R(RMS)}$	35	70	140	280	420	Volts
DC Output Voltage Resistive Load Capactive Load	 Vdc Vdc	 31 50	 62 100	 124 200	 248 400	 372 600	Volts
Average Rectified Forward Current T_A = 25°C T_C = 55°C	I_O	 ← 4.0 → ← 8.0 →					Amp
Nonrepetitive Peak Surge Current (surge applied at rated load conditions, T_J = 150°C)	I_{FSM}	← 100 →					Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	← −65 to +150 →					°C

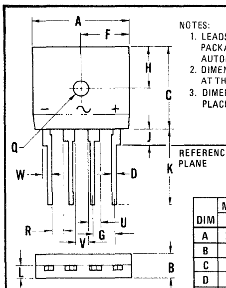
THERMAL CHARACTERISTICS

Characteristics		Symbol	Max (Per Die)	Unit
Thermal Resistance, Junction to Case	Each Die	$R_{\theta JC}$	10	°C/W
	Effective Bridge	$R_{\theta(EFF)}$	7.75	°C/W

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Instaneous Forward Voltage (Per Diode) (i_F = 6.28 Amp, T_J = 25°C) (i_F = 6.28 Amp, T_J = 150°C)	v_F	— — —	 1.1 1.0	Vdc
Reverse Current (Rated V_{RM} applied to ac terminals, + and − terminals open, T_A = 25°C)	I_R	—	1.0	mA

CASE: Transfer-molded plastic encapsulation.
FINISH: All external surfaces are corrosion-resistant. Leads are readily solderable.
POLARITY: Embossed symbols
AC input = ~ DC output = + DC output = −
MOUNTING POSITION: Any
WEIGHT (Approximately): 7.5 Grams
MOUNTING TORQUE: 5 in.-lb. Max



NOTES:
1. LEADS ARE SQUARE AND OFFSET ON PACKAGE (DIM L) TO ALLOW FOR AUTOMATED EQUIPMENT LOADING.
2. DIMENSIONS G & L SHALL BE MEASURED AT THE REFERENCE PLANE.
3. DIMENSIONS R, W AND U APPLY TWO PLACES.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.35	23.37	0.880	0.920
B	6.35	7.37	0.250	0.290
C	18.54	19.56	0.730	0.770
D	0.89	1.14	0.035	0.045
F	11.18	11.68	0.440	0.460
G	4.57	5.59	0.180	0.220
H	8.89	9.91	0.350	0.390
J	2.79	3.81	0.110	0.150
K	14.61	–	0.575	–
L	3.18	3.43	0.125	0.135
Q	3.56	4.06	0.140	0.160
R	2.66 NOM		0.105 NOM	
U	2.66	3.17	0.105	0.125
V	2.92 NOM		0.115 NOM	
W	1.90	2.41	0.075	0.095

CASE 117A-02

FIGURE 1 — FORWARD VOLTAGE

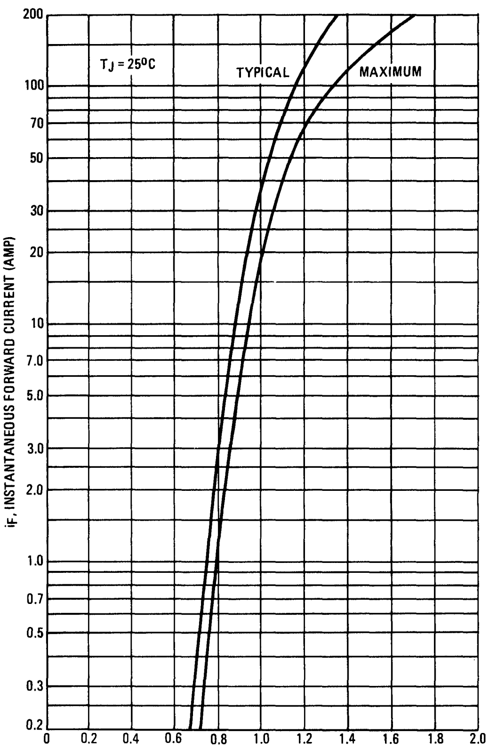


FIGURE 2 — MAXIMUM SURGE CAPABILITY

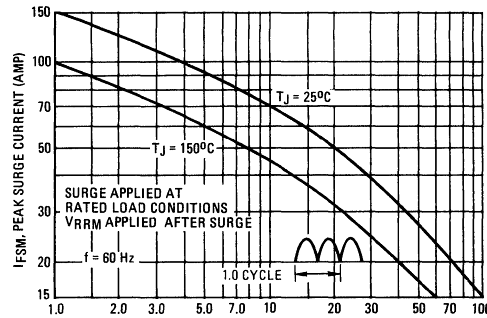


FIGURE 3 — FORWARD VOLTAGE TEMPERATURE COEFFICIENT

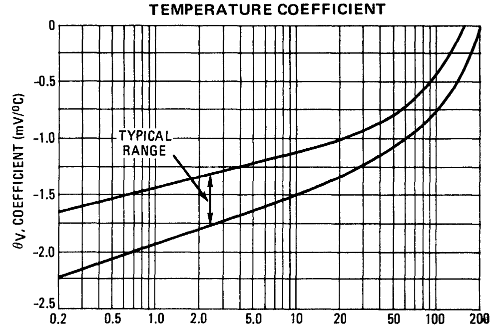
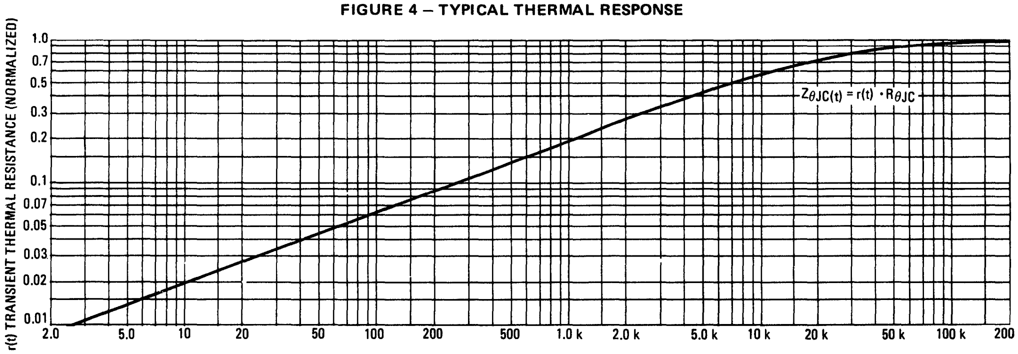


FIGURE 4 — TYPICAL THERMAL RESPONSE



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MAXIMUM CURRENT RATINGS, BRIDGE OPERATION

FIGURE 5 — CASE TEMPERATURE DERATING

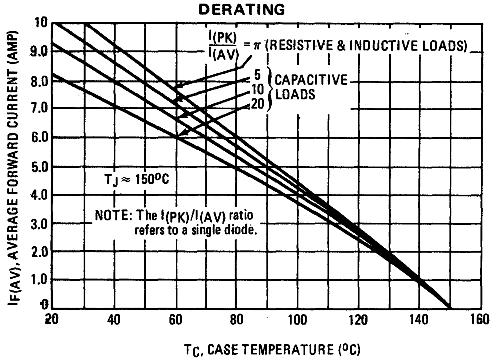
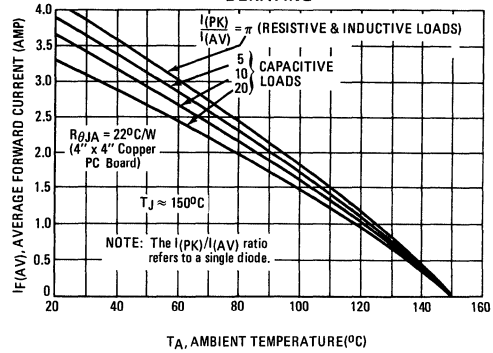


FIGURE 6 — AMBIENT TEMPERATURE DERATING



TYPICAL DYNAMIC CHARACTERISTICS (EACH DIODE)

FIGURE 7 — RECTIFICATION EFFICIENCY

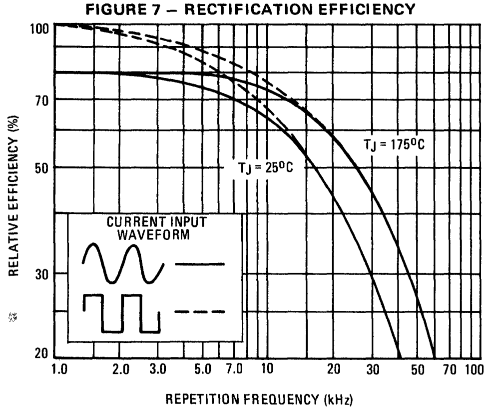


FIGURE 8 — REVERSE RECOVERY TIME

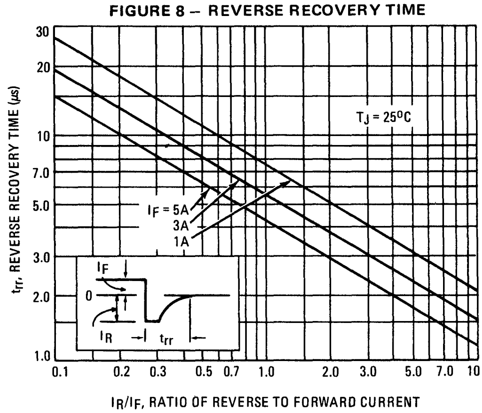


FIGURE 9 — JUNCTION CAPACITANCE

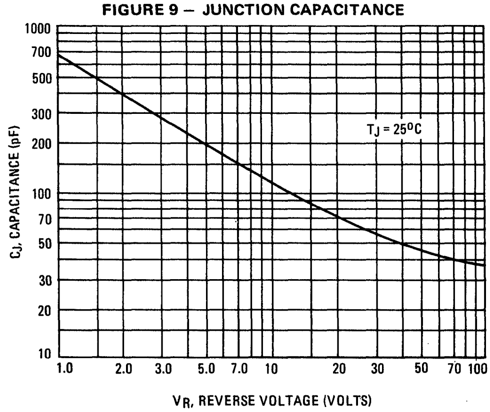


FIGURE 10 — FORWARD RECOVERY TIME

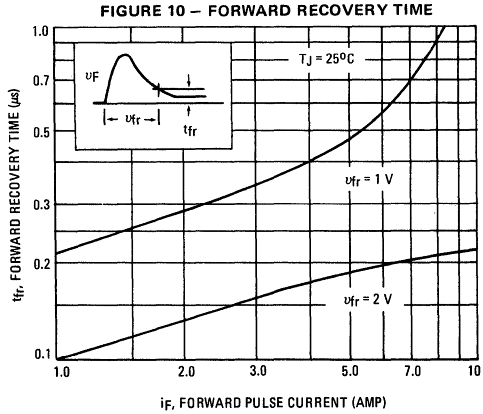


FIGURE 11 – POWER DISSIPATION

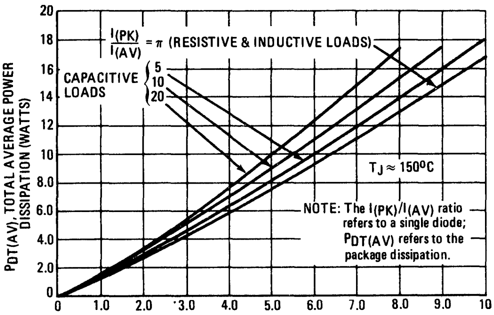
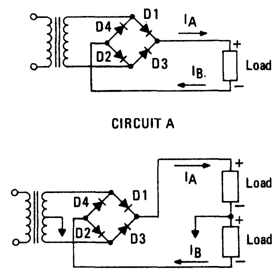


FIGURE 12 – BASIC CIRCUIT USES FOR BRIDGE RECTIFIERS



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NOTE 1: THERMAL COUPLING AND EFFECTIVE THERMAL RESISTANCE

In multiple chip devices where there is coupling of heat between die, the junction temperature can be calculated as follows:

(1) $\Delta T_{J1} = R_{\theta 1} P_{D1} + R_{\theta 2} K_{\theta 2} P_{D2} + R_{\theta 3} K_{\theta 3} P_{D3} + R_{\theta 4} K_{\theta 4} P_{D4}$

Where ΔT_{J1} is the change in junction temperature of diode 1
$R_{\theta 1}$ thru 4 is the thermal resistance of diodes 1 through 4
P_{D1} thru 4 is the power dissipated in diodes 1 through 4
$K_{\theta 2}$ thru 4 is the thermal coupling between diode 1 and diodes 2 through 4.

An effective package thermal resistance can be defined as follows:

(2) $R_{\theta(EFF)} = \Delta T_{J1}/P_{DT}$

where: P_{DT} is the total package power dissipation.

Assuming equal thermal resistance for each die, equation (1) simplifies to

(3) $\Delta T_{J1} = R_{\theta 1}(P_{D1} + K_{\theta 2} P_{D2} + K_{\theta 3} P_{D3} + K_{\theta 4} P_{D4})$

For the conditions where $P_{D1} = P_{D2} = P_{D3} = P_{D4}$, $P_{DT} = 4\, P_D$ equation (3) can be further simplified and by substituting into equation (2) results in

(4) $R_{\theta(EFF)} = R_{\theta 1}(1 + K_{\theta 2} + K_{\theta 3} + K_{\theta 4})/4$

For this rectifier assembly, thermal coupling between opposite diodes is 65% and between adjacent diodes is 72.5% when the case temperature is used as a reference. When the ambient temperature is used as the reference, the coupling is a function of the mounting conditions and is essentially the same for opposite and adjacent diodes.

The effective bridge thermal resistance, junction to ambient, is (from equation 4).

(5) $R_{\theta(EFF)JA} = R_{\theta JA}(1 + 3K_{\theta(AV)JA})/4$

Where: $K_{\theta(AV)JA} \approx (K_{\theta(AV)JC} R_{\theta JC} + R_{\theta CA})/R_{\theta JA}$ and $K_{\theta(AV)JC}$ is approximately 70%. $R_{\theta CA}$ is the case to ambient thermal resistance.

NOTE 2: SPLIT LOAD DERATING INFORMATION

Bridge rectifiers are used in two basic configurations as shown by circuits A and B of Figure 12. The current derating data of Figures 5 and 6 apply to the standard bridge circuit (A) where $I_A = I_B$. For circuit B where $I_A \neq I_B$, derating information can be calculated as follows:

(6) $T_{R(MAX)} = T_{J(MAX)} - \Delta T_{J1}$

Where $T_{R(MAX)}$ is the reference temperature (either case or ambient)

ΔT_{J1} can be calculated using equation (3) in Note 1.

For example, to determine $T_{C(MAX)}$ for the following load conditions:

I_A = 3.1 A average with a peak of 11.2 A
I_B = 1.55 A average with a peak of 6.8 A

First calculate the peak to average ratio for I_A. $I_{(PK)}/I_{(AV)}$ = 11.2/1.55 = 7.23 (Note that the peak to average ratio is on a per diode basis.)

From Figure 11, for an average current of 3.1 A and an $I_{(PK)}/I_{(AV)}$ = 7.23 read $P_{T(AV)}$ = 4.8 watts or 1.2 watts/diode ∴ $P_{D1} = P_{D3}$ = 1.2 watts.

Similarly, for a load current I_B of 1.55 A, diode #2 and diode #4 each see 0.775 A average resulting in an $I_{(PK)}/I_{(AV)} \approx 8.8$.

Thus, the package power dissipation for 1.55 A is 2.3 watts or 0.575 watts/diode ∴ $P_{D2} = P_{D4}$ = 0.575 watts.

The maximum junction temperature occurs in diode #1 and #3. From equation (3) for diode #1 ΔT_{J1} = 9[1.2 +.65(.575) +.725 (1.2) + .725 (.575)]

$\Delta T_{J1} \approx 26°C$

Thus $T_{C(MAX)}$ = 150-26 = 124°C

The total package dissipation in this example is:

$P_J = 2 \times 1.2 + 2 \times 0.575 \approx 3.6$ watts

(Note that although maximum $R_{\theta JC}$ is 10°C/watt, 9°C/watt is used in this example and on the derating data as it is unlikely that all four die in a given package would be at the maximum value.)

NOTE 3

Under typical wire terminal or printed circuit board mounting conditions, the thermal resistance between the diode junctions and the leads at the edge of the case is a small fraction of the thermal resistance from junction to ambient. Consequently, the lead temperature is very close to the junction temperature. Therefore, it is recommended that the lead temperature be measured when the diodes are operating in prototype equipment, in order to determine if operation is within the diode temperature ratings. The lead having the highest thermal resistance to the ambient will yield readings closest to the junction temperature. By measuring temperature as outlined, variations of junction to ambient thermal resistance, caused by the amount of surface area of the terminals or printed circuit board and the degree of air convection, as well as proximity of other heat sources cease to be important design considerations.