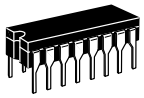
Universal Decade Counter

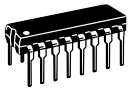
MC10137

The MC10137 is a high speed synchronous counter that can count up, down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the MC10137 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. Carry Out goes low on the terminal count. The Carry Out on the MC10137 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the Carry Out after the Clock's positive excursion will depend on the condition of Q1 and/or Q2. The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.



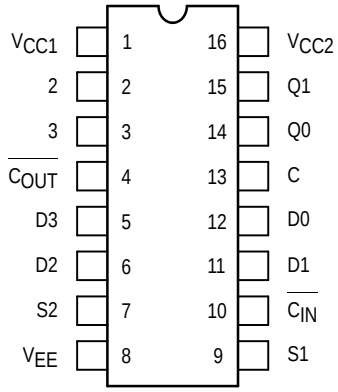
L SUFFIX
CERAMIC PACKAGE
CASE 620–10



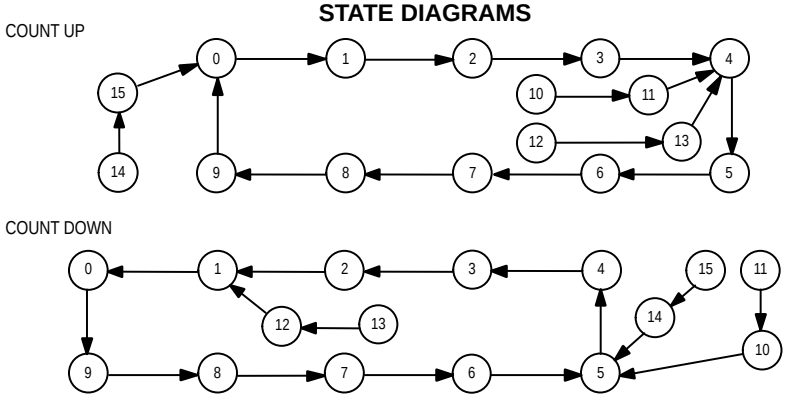
P SUFFIX
PLASTIC PACKAGE
CASE 648–08

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ
t_{pd} = 3.3 ns typ (C–Q)
= 7.0 ns typ (C–C_{out})
= 5.0 ns typ (C_{in}–C_{out})

PIN ASSIGNMENT



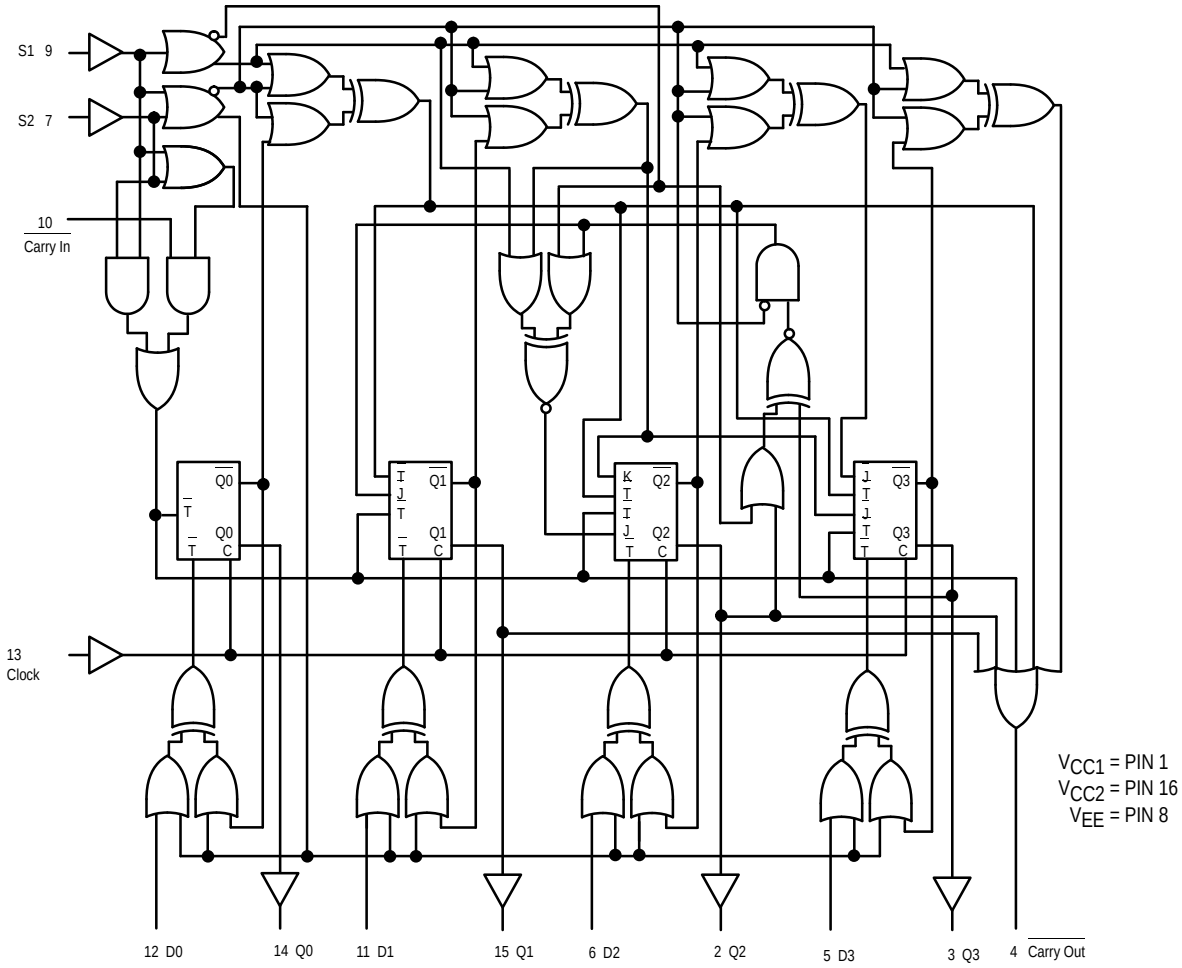
STATE DIAGRAMS



FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

LOGIC DIAGRAM



NOTE: Flip–flops will toggle when all $\overline{T}$ inputs are low.

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry}}$ In	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry}}$ Out
L	L	H	H	H	L	X	H	H	H	H	L	H
L	H	X	X	X	X	L	H	L	L	L	H	H
L	H	X	X	X	X	L	H	H	L	L	H	L
L	H	X	X	X	X	L	H	L	L	L	L	H
L	H	X	X	X	X	L	H	H	L	L	L	H
L	H	X	X	X	X	H	L	H	L	L	L	H
L	H	X	X	X	X	H	H	H	L	L	L	H
H	H	X	X	X	X	X	H	H	L	L	L	H
L	L	H	H	L	L	X	H	H	H	L	L	H
H	L	X	X	X	X	L	H	L	H	L	L	H
H	L	X	X	X	X	L	H	H	L	L	L	H
H	L	X	X	X	X	L	H	L	L	L	L	L

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.
** A clock H is defined as a clock input transition from a low to a high logic level.

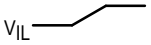
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	Test Limits							Unit
			–30°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	8		165		120	150		165	mAdc
Input Current	I_{inH}	5,6,11,12 7 9,10 13		350 425 390 460			220 265 245 290		220 265 245 290	µAdc
	I_{inL}	All	0.5		0.5			0.3		µAdc
Output Voltage Logic 1	V_{OH}	14 (2.)	–1.060	–0.890	–0.960		–0.810	–0.890	–0.700	Vdc
Output Voltage Logic 0	V_{OL}	14 (2.)	–1.890	–1.675	–1.850		–1.650	–1.825	–1.615	Vdc
Threshold Voltage Logic 1	V_{OHA}	14 (2.)	–1.080		–0.980			–0.910		Vdc
Threshold Voltage Logic 0	V_{OLA}	14 (2.)		–1.655			–1.630		–1.595	Vdc
Switching Times (50Ω Load)										ns
Propagation Delay Clock Input	t_{13+14+} t_{13+14-} t_{13+4+} t_{13+4-}	14 14 4 4	0.8 0.8 2.0 2.0	4.8 4.8 10.9 10.9	1.0 1.0 2.5 2.5	3.3 3.3 7.0 7.0	4.5 4.5 10.5 10.5	1.1 1.1 2.4 2.4	5.0 5.0 11.5 11.5	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{10-4-} t_{10+4+}	4 (3.) 4	1.6 1.6	7.4 7.4	1.6 1.6	5.0 5.0	6.9 6.9	1.9 1.9	7.5 7.5	
Setup Time Data Inputs	t_{12+13+} t_{12-13+}	14 14	3.5 3.5		3.5 3.5			3.5 3.5		
Select Inputs	t_{9+13+} t_{7+13+}	14 14	7.5 7.5		7.5 7.5			7.5 7.5		
$\overline{\text{Carry In}}$ Input	t_{10-13+} t_{13+10+}	14 14	4.5 –1.0		3.7 –1.0			4.5 –1.0		
Hold Time Data Inputs	t_{13+12+} t_{13+12-}	14 14	0 0		0 0			0 0		
Select Inputs	t_{13+9+} t_{13+7+}	14 14	–2.5 –2.5		–2.5 –2.5			–2.5 –2.5		
$\overline{\text{Carry In}}$ Input	t_{13+10-} t_{10+13+}	14 14	–1.6 4.0		–1.6 3.1			–1.6 4.0		
Counting Frequency	$f_{countup}$ $f_{countdown}$	14 14	125 125		125 125	150 150		125 125		MHz
Rise Time (20 to 80%)	t_{4+} t_{14+}	4 14	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	ns
Fall Time (20 to 80%)	t_{4-} t_{14-}	4 14	0.9 0.9	3.3 3.3	1.1 1.1	2.0 2.0	3.3 3.3	1.1 1.1	3.5 3.5	

1. Individually apply V_{ILmin} to pin under test.
2. Measure output after clock pulse V_{IL} ⟋ V_{IH} appears at clock input (Pin 13).
3. Before test set Q1 and Q2 outputs to a logic low.

ELECTRICAL CHARACTERISTICS (continued)

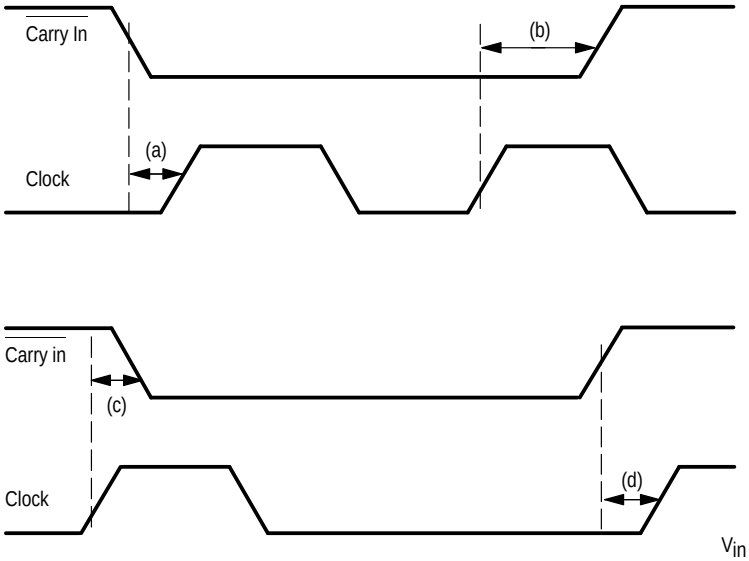
				TEST VOLTAGE VALUES (Volts)					
			@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
			–30°C	–0.890	–1.890	–1.205	–1.500	–5.2	
			+25°C	–0.810	–1.850	–1.105	–1.475	–5.2	
			+85°C	–0.700	–1.825	–1.035	–1.440	–5.2	
Characteristic		**Symbol**	**Pin Under Test**	**TEST VOLTAGE APPLIED TO PINS LISTED BELOW**					**(V_{CC}) Gnd**
				V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	
Power Supply Drain Current		I_E	8					8	1, 16
Input Current		I_{inH}	5,6,11,12	5,6,11,12				8	1, 16
			7	7				8	1, 16
			9,10	9,10				8	1, 16
			13	13				8	1, 16
		I_{inL}	All		Note 1.			8	1, 16
Output Voltage	Logic 1	V_{OH}	14 (2.)	12	7, 9			8	1, 16
Output Voltage	Logic 0	V_{OL}	14 (2.)		7, 9			8	1, 16
Threshold Voltage	Logic 1	V_{OHA}	14 (2.)		7, 9	12		8	1, 16
Threshold Voltage	Logic 0	V_{OLA}	14 (2.)		7, 9		12	8	1, 16
Switching Times	(50Ω Load)			**+1.11V**	**+0.31V**	**Pulse In**	**Pulse Out**	**–3.2 V**	**+2.0 V**
Propagation Delay	Clock Input	t_{13+14+}	14	12		13	14	8	1, 16
		t_{13+14-}	14			13	14	8	1, 16
		t_{13+4+}	4	7		13	4	8	1, 16
		t_{13+4-}	4	7		13	4	8	1, 16
	$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	t_{10-4-}	4 (3.)	7	13	10	4	8	1, 16
		t_{10+4+}	4	7	13	10	4	8	1, 16
Setup Time	Data Inputs	t_{12+13+}	14		7, 9	12, 13	14	8	1, 16
		t_{12-13+}	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t_{9+13+}	14			9, 13	14	8	1, 16
		t_{7+13+}	14			7, 13	14	8	1, 16
	$\overline{\text{Carry In}}$ Inputs	t_{10-13+}	14	7	9	10, 13	14	8	1, 16
		t_{13+10+}	14	7	9	10, 13	14	8	1, 16
Hold Time	Data Inputs	t_{13+12+}	14		7, 9	12, 13	14	8	1, 16
		t_{13+12-}	14		7, 9	12, 13	14	8	1, 16
	Select Inputs	t_{13+9+}	14			9, 13	14	8	1, 16
		t_{13+7+}	14			7, 13	14	8	1, 16
	$\overline{\text{Carry In}}$ Inputs	t_{13+10-}	14	7	9	10, 13	14	8	1, 16
		t_{10+13+}	14	7	9	10, 13	14	8	1, 16
Counting Frequency		$f_{countup}$	14	7		13	14	8	1, 16
		$f_{countdown}$	14	9		13	14	8	1, 16
Rise Time	(20 to 80%)	t_{4+}	4	7		13	4	8	1, 16
		t_{14+}	14	7		13	14	8	1, 16
Fall Time	(20 to 80%)	t_{4-}	4	7		13	4	8	1, 16
		t_{14-}	14	7		13	14	8	1, 16

1. Individually test each input; apply V_{ILmin} to pin under test.
2. Measure output after clock pulse  appears at clock input (Pin 13).

3. Before test set all Q outputs to a logic high.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

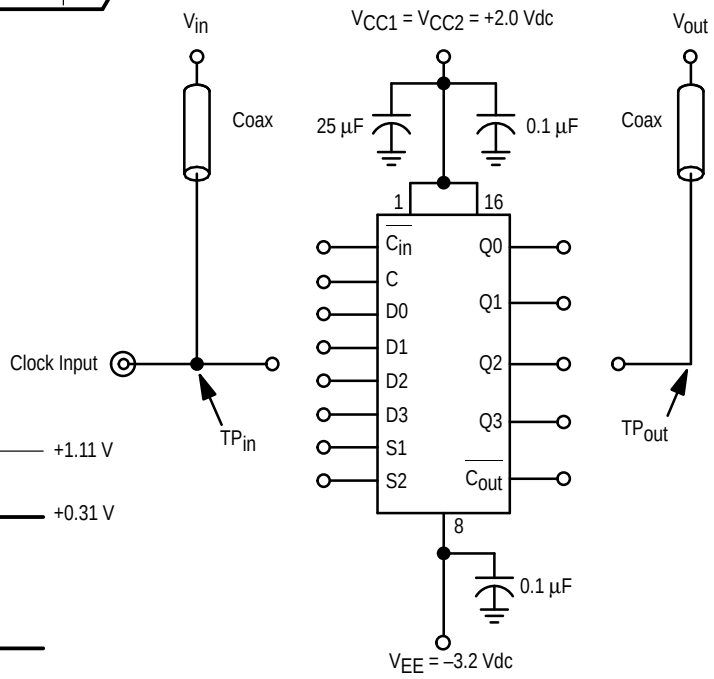
(b) and (c) may be negative numbers.

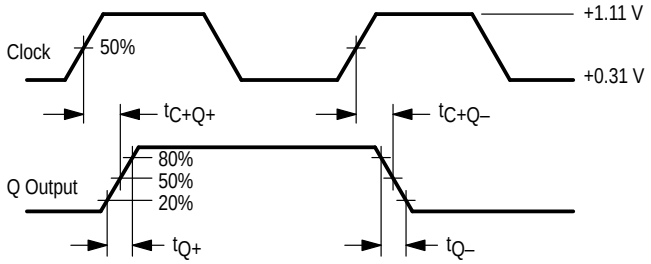
NOTE:

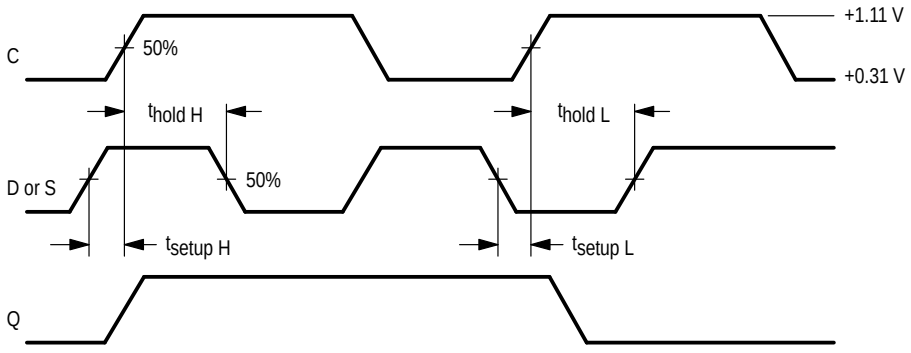
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

Input Pulse
t+ = t– = 2.0 ±0.2 ns
(20 to 80%)







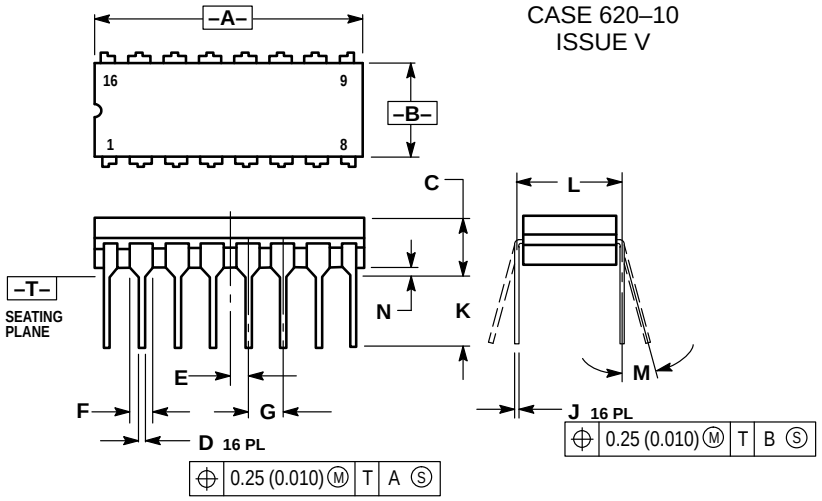
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Unused outputs are connected to a 50-ohm resistor to ground.

OUTLINE DIMENSIONS

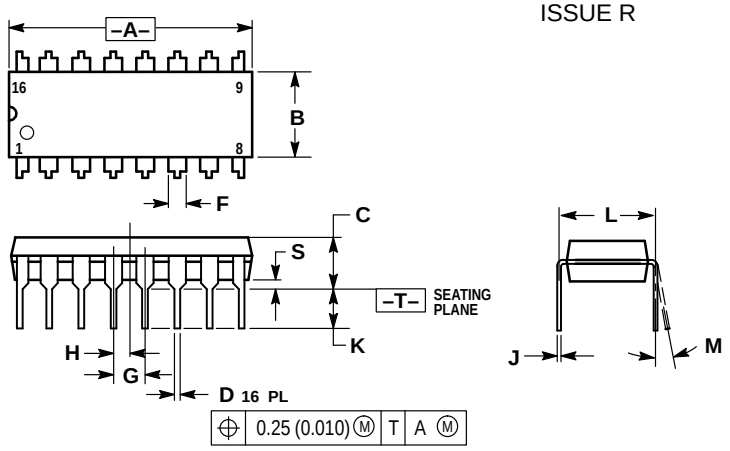
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0 °	15 °	0 °	15 °
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

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