

IRFD1Z0, IRFD1Z1 IRFD1Z2, IRFD1Z3

N-Channel Enhancement-Mode
Power Field-Effect Transistors

August 1991

Features

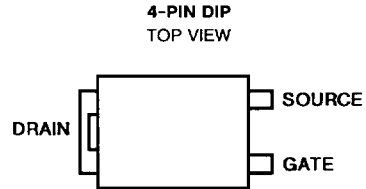
- 0.4A and 0.5A, 60V - 100V
- $r_{DS(on)} = 2.4\Omega$ and 3.2Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The IRFD1Z0, IRFD1Z1, IRFD1Z2, and IRFD1Z3 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

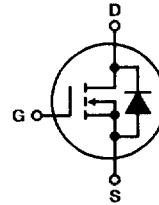
The IRFD types are supplied in the 4-pin DIP package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



N-CHANNEL
POWER MOSFETS

Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$), Unless Otherwise Specified

	IRFD1Z0	IRFD1Z1	IRFD1Z2	IRFD1Z3	UNITS
Drain-Source Voltage (1)	V_{DS} 100	60	100	60	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} 100	60	100	60	V
Continuous Drain Current					
$T_C = +25^\circ\text{C}$	I_D 0.5	0.5	0.4	0.4	A
Pulsed Drain Current	I_{DM} 4.0	4.0	3.2	3.2	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation					
$T_C = +25^\circ\text{C}$ (See Figure 13)	P_D 1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/ $^\circ\text{C}$
Inductive Current, Clamped	I_{LM} 4.0	4.0	3.2	3.2	A
(See Figures 14 and 15, L 100 μH)					
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

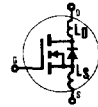
1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$.
2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.

Specifications IRFD1Z0, IRFD1Z1, IRFD1Z2, IRFD1Z3

Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV _{DSS} Drain - Source Breakdown Voltage	IRFD1Z0, 2	100	—	—	V	V _{GS} = 0V
	IRFD1Z1, 3	60	—	—	V	I _D = 250μA
V _{GS(th)} Gate Threshold Voltage	ALL	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{GSS} Gate - Source Leakage Forward	ALL	—	—	500	nA	V _{GS} = 20V
I _{GSS} Gate - Source Leakage Reverse	ALL	—	—	-500	nA	V _{GS} = -20V
I _{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	V _{DS} = Max. Rating, V _{GS} = 0V
		—	—	1000	μA	V _{DS} = Max. Rating x 0.8, V _{GS} = 0V, T _C = 125°C
I _{D(on)} On-State Drain Current ②	IRFD1Z0, 1	0.5	—	—	A	V _{DS} > I _{D(on)} × R _{DS(on)} max., V _{GS} = 10V
	IRFD1Z2, 3	0.4	—	—	A	
R _{DS(on)} Static Drain-Source On-State Resistance ②	IRFD1Z0, 1	—	2.2	2.4	Ω	V _{GS} = 10V, I _D = 0.25A
	IRFD1Z2, 3	—	2.8	3.2	Ω	
g _{fs} Forward Transconductance ②	ALL	0.25	0.35	—	S (Ω)	V _{DS} > I _{D(on)} × R _{DS(on)} max., I _D = 0.25A
C _{iss} Input Capacitance	ALL	—	50	—	pF	V _{GS} = 0V, V _{DS} = 25V, f = 1.0 MHz See Fig. 9
C _{oss} Output Capacitance	ALL	—	20	—	pF	
C _{rss} Reverse Transfer Capacitance	ALL	—	5.0	—	pF	
t _{d(on)} Turn-On Delay Time	ALL	—	10	20	ns	V _{DD} = 0.5 BV _{DSS} , I _D = 0.25A, Z _o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t _r Rise Time	ALL	—	15	25	ns	
t _{d(off)} Turn-Off Delay Time	ALL	—	15	25	ns	
t _f Fall Time	ALL	—	10	20	ns	
Q _g Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	—	2.0	3.0	nC	
Q _{gs} Gate-Source Charge	ALL	—	1.0	—	nC	V _{GS} = 10V, I _D = 1.2A, V _{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q _{gd} Gate-Drain ("Miller") Charge	ALL	—	1.0	—	nC	
L _D Internal Drain Inductance	ALL	—	4.0	—	nH	
L _S Internal Source Inductance	ALL	—	6.0	—	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Thermal Resistance

R _{thJA} Junction-to-Ambient	ALL	—	—	120	°C/W	Free Air Operation
---------------------------------------	-----	---	---	-----	------	--------------------

Source-Drain Diode Ratings and Characteristics

I _S Continuous Source Current (Body Diode)	IRFD1Z0, 1	—	—	0.5	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRFD1Z2, 3	—	—	0.4	A	
I _{SM} Pulse Source Current (Body Diode)	IRFD1Z0, 1	—	—	4.0	A	
	IRFD1Z2, 3	—	—	3.2	A	
V _{SD} Diode Forward Voltage ②	IRFD1Z0, 1	—	—	1.4	V	T _A = 25°C, I _S = 0.5A, V _{GS} = 0V
	IRFD1Z2, 3	—	—	1.3	V	T _A = 25°C, I _S = 0.4A, V _{GS} = 0V
t _{rr} Reverse Recovery Time	ALL	—	100	—	ns	T _J = 150°C, I _F = 0.5A, dI _F /dt = 100A/μs
Q _{RR} Reverse Recovered Charge	ALL	—	0.2	—	μC	T _J = 150°C, I _F = 0.5A, dI _F /dt = 100A/μs
t _{on} Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

① T_J = 25°C to 150°C.

② Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

IRFD120, IRFD121, IRFD122, IRFD123

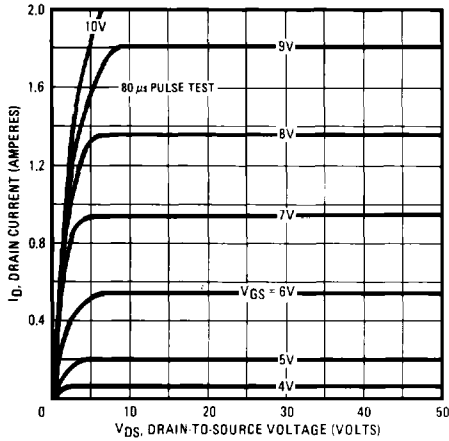


Fig. 1 - Typical Output Characteristics

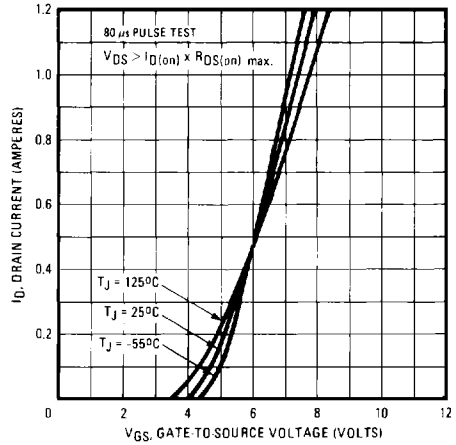


Fig. 2 - Typical Transfer Characteristics

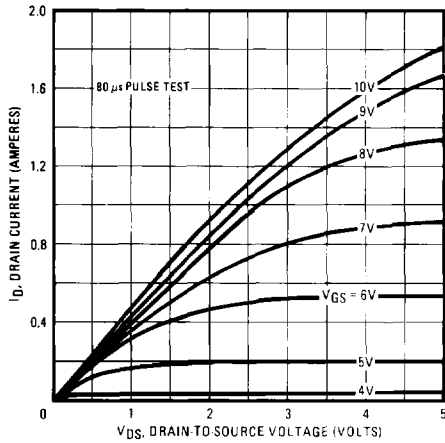


Fig. 3 - Typical Saturation Characteristics

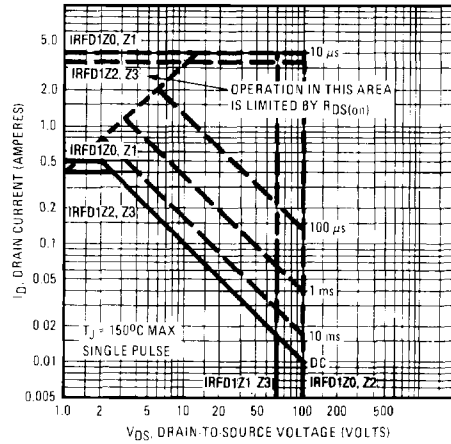


Fig. 4 - Maximum Safe Operating Area

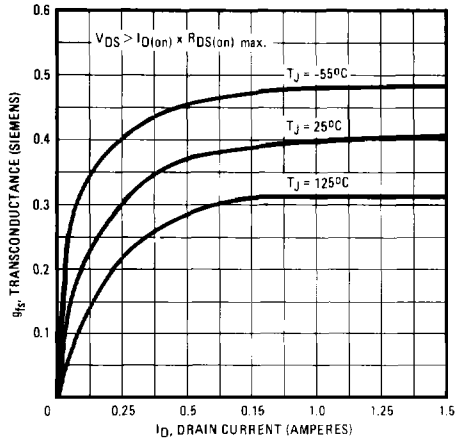


Fig. 5 - Typical Transconductance Vs. Drain Current

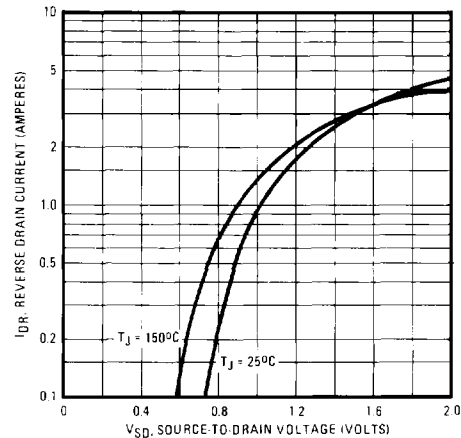


Fig. 6 - Typical Source-Drain Diode Forward Voltage

N-CHANNEL
POWER MOSFETS

IRFD1Z0, IRFD1Z1, IRFD1Z2, IRFD1Z3

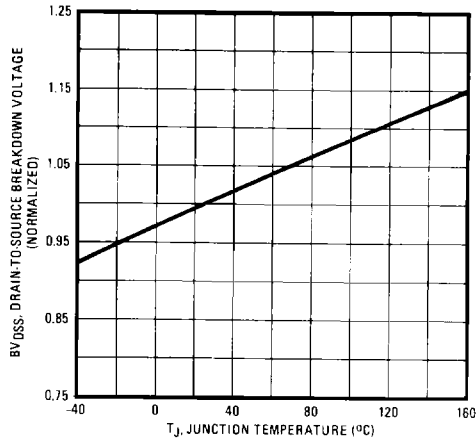


Fig. 7 – Breakdown Voltage Vs. Temperature

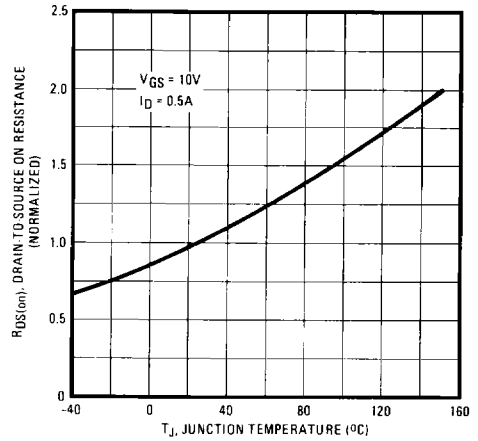


Fig. 8 – Normalized On-Resistance Vs. Temperature

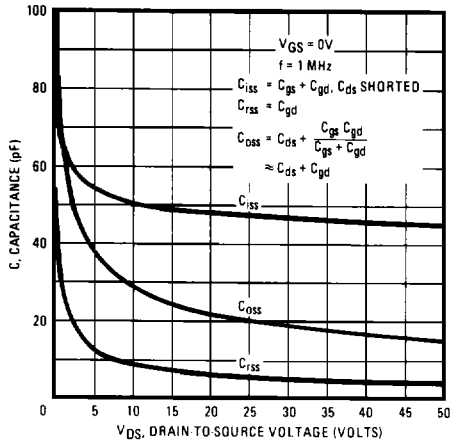


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

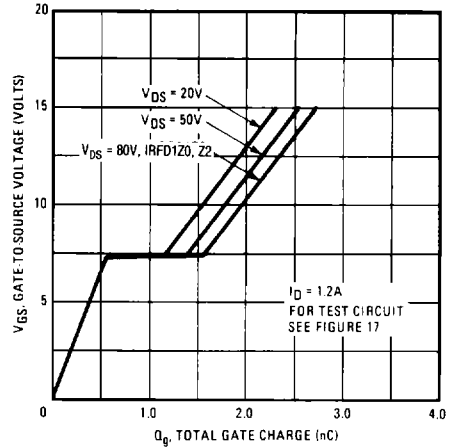


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

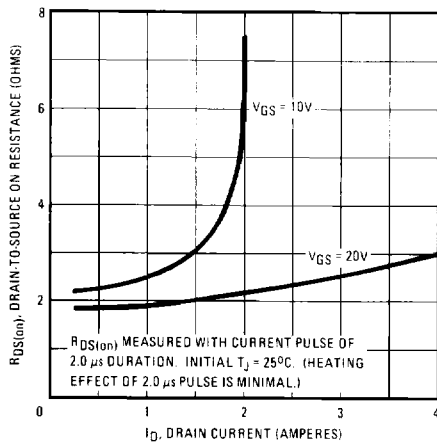


Fig. 11 – Typical On-Resistance Vs. Drain Current

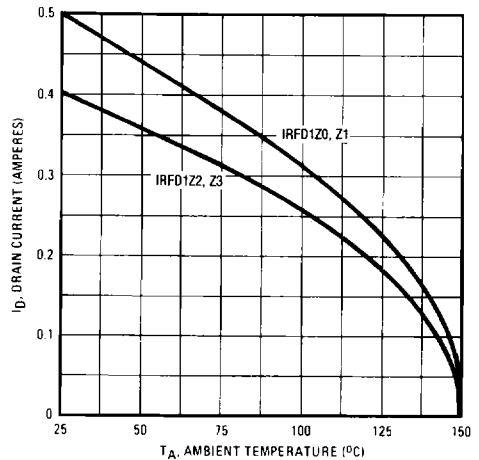


Fig. 12 – Maximum Drain Current Vs. Case Temperature

IRFD120, IRFD121, IRFD122, IRFD123

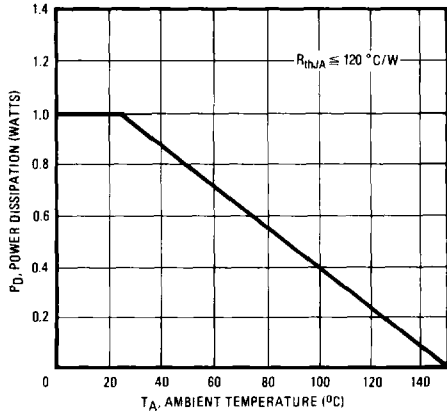


Fig. 13 - Power Vs. Temperature Derating Curve

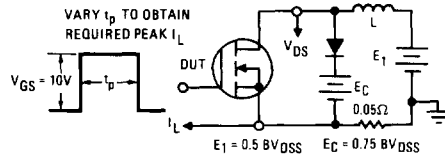


Fig. 14 - Clamped Inductive Test Circuit

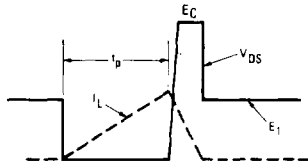


Fig. 15 - Clamped Inductive Waveforms

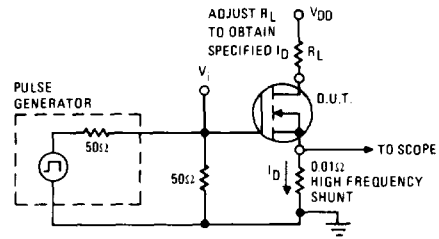


Fig. 16 - Switching Time Test Circuit

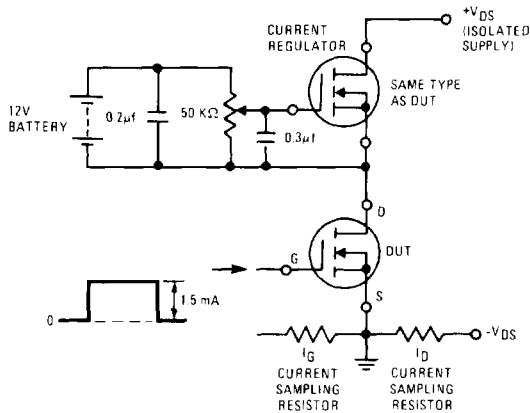


Fig. 17 - Gate Charge Test Circuit