

August 1991

Features

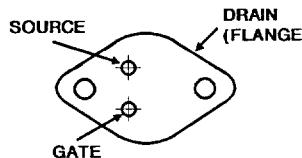
- 21A and 19A, 500V
- $r_{DS(on)} = 0.27\Omega$ and 0.35Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

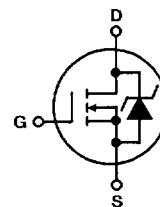
The IRF460 and IRF462 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF-types are supplied in the JEDEC TO-204AE metal package.

Package

 TO-204AE
BOTTOM VIEW

Terminal Diagram

N-CHANNEL ENHANCEMENT MODE


Absolute Maximum Ratings ($T_C = +25^\circ C$), Unless Otherwise Specified

	IRF460	IRF462	UNITS
Continuous Drain Current			
$T_C = +25^\circ C$	I_D	21	A
$T_C = +100^\circ C$	I_D	14	A
Pulsed Drain Current (1)	I_{DM}	84	A
Gate-Source Voltage	V_{GS}	± 20	V
Maximum Power Dissipation			
$T_C = +25^\circ C$	P_D	300	W
Linear Derating Factor		2.4	$W/^\circ C$
Single Pulse Avalanche Energy Rating (2)	E_{AS}^*	1200	mJ
See Figure 14			
Avalanche Current, Repetitive or Non-repetitive (1)	I_{AR}	21	A
Operating and Storage Junction	T_J, T_{STG}	-55 to +150	$^\circ C$
Temperature Range			
Maximum Lead Temperature for Soldering	T_L	300	$^\circ C$
(0.063" (1.6mm) from case for 10s)			

NOTES:

1. Repetitive rating: Pulse width limited by maximum junction temperature.
See Transient Thermal Impedance Curve (Figure 5).
2. $V_{DD} = 50V$, starting $T_J = +25^\circ C$, $L = 4.9mH$, $R_{GS} = 25\Omega$. Peak $I_L = 21A$.
3. Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

IRF460, IRF462

ELECTRICAL CHARACTERISTICS At Case Temperature (T_J) = 25°C Unless Otherwise Specified

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
V_{DSS} Drain-to-Source Breakdown Voltage	ALL	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$ Static Drain-to-Source On-State Resistance ①	IRF460	—	0.24	0.27	Ω	$V_{GS} = 10V, I_D = 12A$
	IRF462	—	0.27	0.35	Ω	
$I_{D(on)}$ On-State Drain Current ③	IRF460	21	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ Max.}$ $V_{GS} = 10V$
	IRF462	19	—	—	A	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs} Forward Transconductance ③	ALL	13	20	—	S (f)	$V_{DS} \geq 50V, I_{DS} = 12A$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$ $V_{DS} = 0.8 \times \text{Max. Rating}$ $V_{GS} = 0V, T_J = 125^{\circ}\text{C}$
	ALL	—	—	1000	μA	
I_{GSS} Gate-to-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS} Gate-to-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
Q_g Total Gate Charge	ALL	—	120	190	nC	$V_{GS} = 10V, I_D = 21A$
Q_{gs} Gate-to-Source Charge	ALL	—	18	—	nC	$V_{DS} = 0.8 \times \text{Max. Rating}$
Q_{gd} Gate-to-Drain ("Miller") Charge	ALL	—	62	—	nC	See Fig. 16 (Independent of operating temperature)
$t_{d(on)}$ Turn-On Delay Time	ALL	—	23	35	ns	$V_{DD} = 250V, I_D \approx 21A, R_G = 4.3Ω$
t_r Rise Time	ALL	—	81	120	ns	$R_D = 12Ω$
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	85	130	ns	See Fig. 15
t_f Fall Time	ALL	—	65	98	ns	(Independent of operating temperature)
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S Internal Source Inductance	ALL	—	13	—	nH	Modified MOSFET symbol showing the internal inductances. Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss} Input Capacitance	ALL	—	4100	—	pF	$V_{GS} = 0V, V_{DS} = 25V$
C_{oss} Output Capacitance	ALL	—	480	—	pF	$f = 1.0 \text{ MHz}$
C_{rss} Reverse Transfer Capacitance	ALL	—	84	—	pF	See Fig. 10
R_{thJC} Junction-to-Case	ALL	—	—	0.42	°C/W	
R_{thJS} Case-to-Sink	ALL	—	0.10	—	°C/W	Mounting surface flat, smooth, and greased
R_{thJA} Junction-to-Ambient	ALL	—	—	30	°C/W	Typical socket mount

① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 5)
Refer to current HEXFET reliability report

② @ $V_{DD} = 50V$, Starting $T_J = 25^{\circ}\text{C}$,
 $L = 4.9 \mu\text{H}$, $R_G = 25\Omega$,
Peak $I_L = 21A$.

③ Pulse width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2\%$

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	ALL	—	—	21	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier.
I_{SM} Pulsed Source Current (Body Diode) ①	ALL	—	—	84	A	
V_{SD} Diode Forward Voltage ③	ALL	—	—	1.8	V	$T_J = 25^{\circ}\text{C}, I_S = 21A, V_{GS} = 0V$
t_{rr} Reverse Recovery Time	ALL	280	580	1200	ns	$T_J = 25^{\circ}\text{C}, I_F = 21A, dI/dt = 100 \text{ A}/\mu\text{s}$
Q_{RR} Reverse Recovery Charge	ALL	3.8	8.1	18	μC	
t_{on} Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

IRF460, IRF462

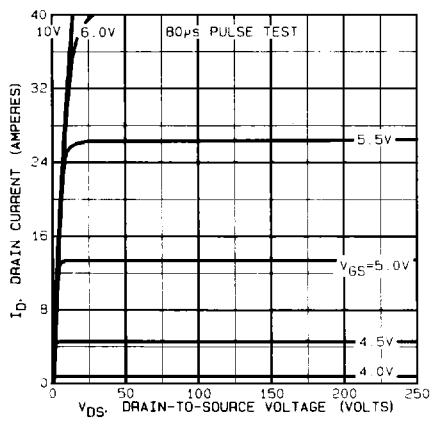


Fig. 1 - Typical output characteristics.

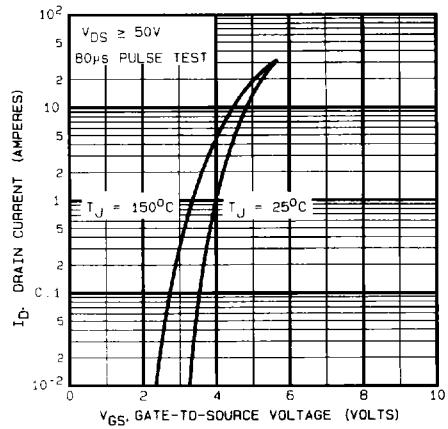


Fig. 2 - Typical transfer characteristics.

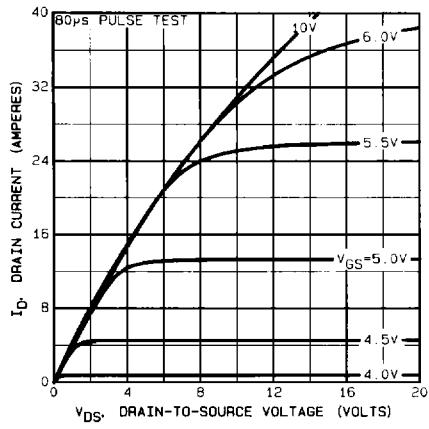


Fig. 3 - Typical saturation characteristics.

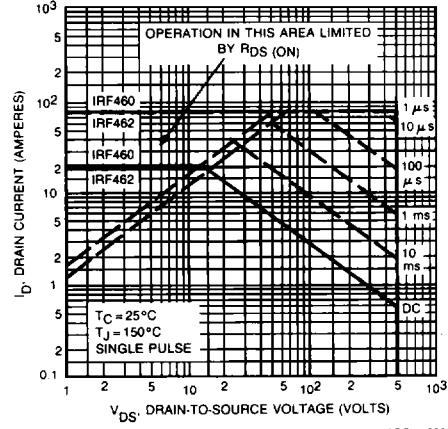


Fig. 4 - Maximum safe operating area.

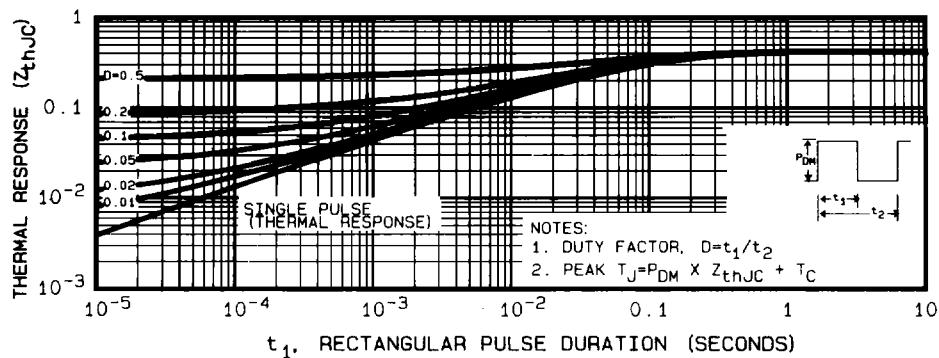


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

IRF460, IRF462

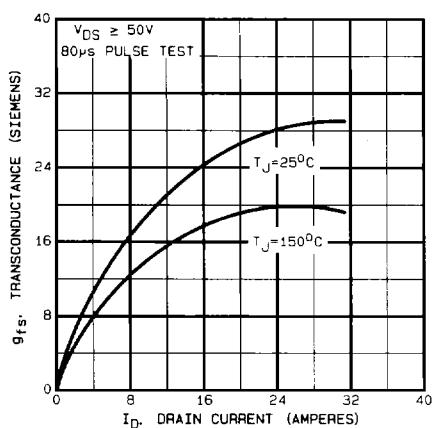


Fig. 6 - Typical transconductance vs. drain current.

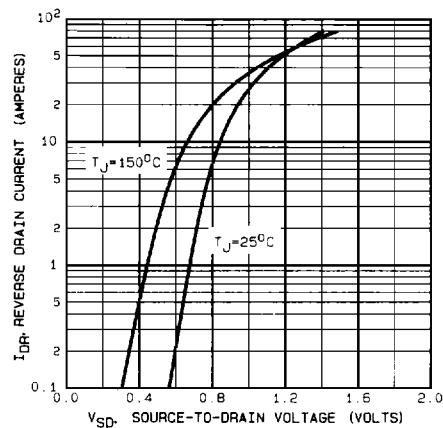


Fig. 7 - Typical source-drain diode forward voltage.

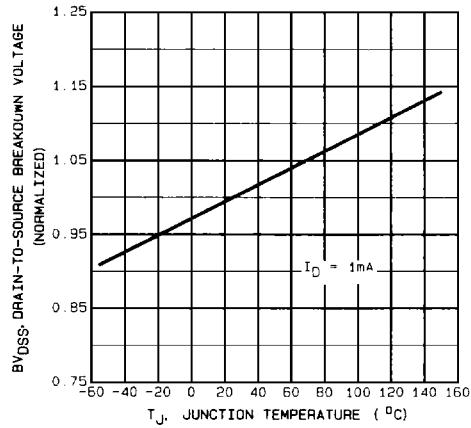


Fig. 8 - Breakdown voltage vs. temperature.

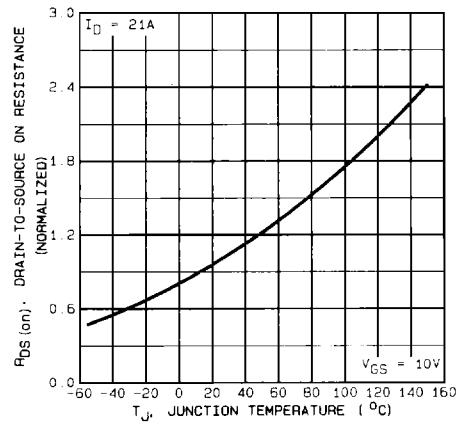


Fig. 9 - Normalized on-resistance vs. temperature.

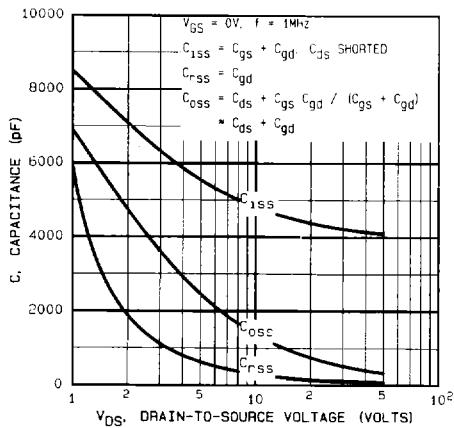


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

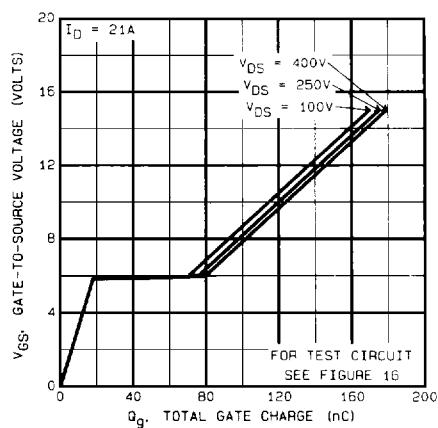


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

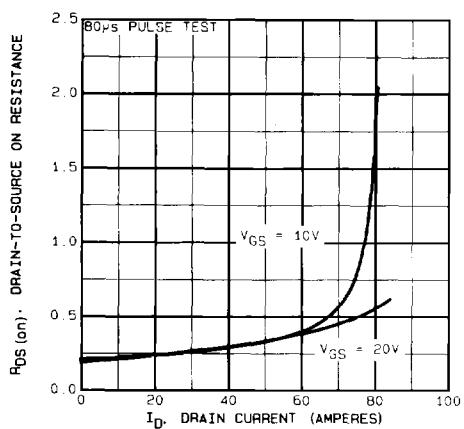


Fig. 12 - Typical on-resistance vs. drain current.

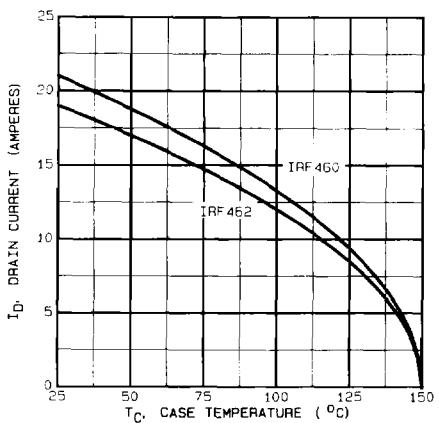


Fig. 13 - Maximum drain current vs. case temperature.

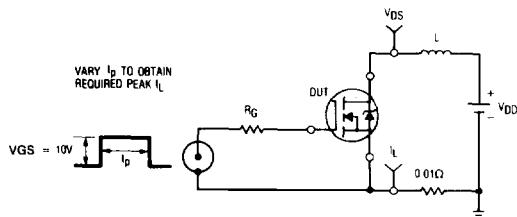


Fig. 14a - Unclamped inductive test circuit.

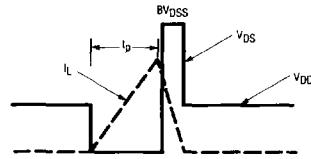


Fig. 14b - Unclamped inductive waveforms.

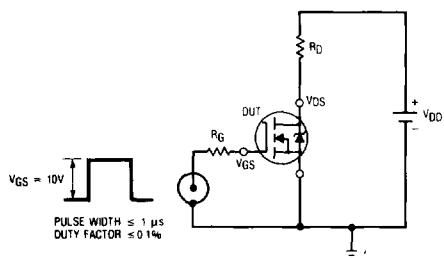


Fig. 15a - Switching time test circuit.

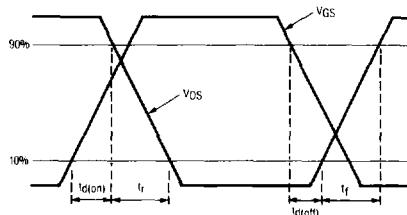


Fig. 15b - Switching time waveforms.

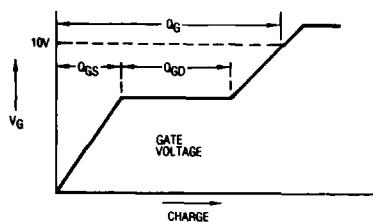


Fig. 16a - Basic gate charge waveform.

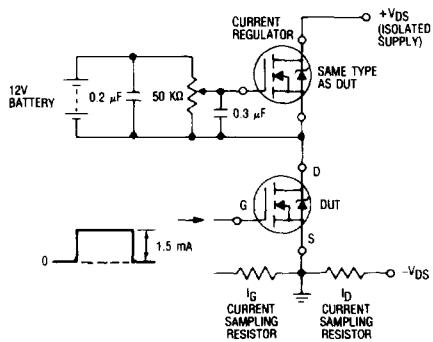


Fig. 16b - Gate charge test circuit.