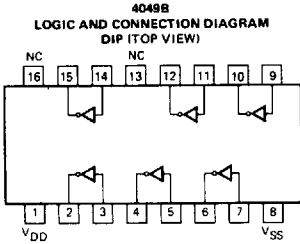


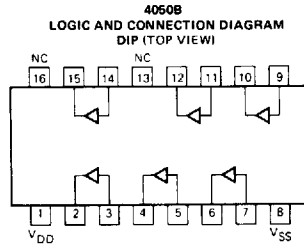
# GD4049B • GD4050B

## 4049B HEX INVERTING BUFFER • 4050B HEX NON-INVERTING BUFFER

**DESCRIPTION** — These CMOS buffers provide high current output capability suitable for driving TTL or high capacitance loads. Since input voltages in excess of the buffers' supply voltage are permitted, these buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. The 4049B provides six inverting buffers, the 4050B six non-inverting buffers. Their guaranteed fan out into common bipolar logic elements is shown in Table 1.



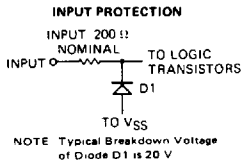
**NOTE**  
The SO Package has the same pinouts (Connection Diagram) as the Dual In line Package



**TABLE 1**  
Guaranteed fan out of 4049B, 4050B into common logic families

DRIVEN ELEMENT	GUARANTEED FAN OUT
Standard TTL, DTL	2
9LS, 93L, 74LS	9
74L	16

Conditions:  $V_{DD} = V_{CC} = 5.0 \pm 0.25 \text{ V}$   
 $V_{OL} = 0.5 \text{ V}$   $T_A = 0 \text{ to } 75^\circ \text{ C}$



**DC CHARACTERISTICS:**  $V_{DD}$  as shown,  $V_{SS} = 0 \text{ V}$ , 4049BXM and 4050BXM (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		$V_{DD} = 5 \text{ V}$			$V_{DD} = 10 \text{ V}$			$V_{DD} = 15 \text{ V}$					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
$I_{OH}$	Output HIGH Current	-1.85									mA	MIN, 25°C MAX	$V_{OUT} = 2.5 \text{ V}$ for $V_{DD} = 5 \text{ V}$ Inputs at 0 or $V_{DD}$ per Function
		-1.25	-2.5										
$I_{OH}$	Output HIGH Current	-0.62			-1.85			-5.5			mA	MIN, 25°C MAX	$V_{OUT} = 4.5 \text{ V}$ for $V_{DD} = 5 \text{ V}$ $V_{OUT} = 9.5 \text{ V}$ for $V_{DD} = 10 \text{ V}$ $V_{OUT} = 13.5 \text{ V}$ for $V_{DD} = 15 \text{ V}$ Inputs at 0 or $V_{DD}$ per Function
		-0.5	-1		-1.25	-2.5		-3.75	-7.5	-2.7			
$I_{OL}$	Output LOW Current	3.75			10			30			mA	MIN, 25°C MAX	$V_{OUT} = 0.4 \text{ V}$ for $V_{DD} = 5 \text{ V}$ $V_{OUT} = 0.5 \text{ V}$ for $V_{DD} = 10 \text{ V}$ $V_{OUT} = 1.5 \text{ V}$ for $V_{DD} = 15 \text{ V}$ Inputs at 0 or $V_{DD}$ per Function
		3	6		8	16		24	48	16.8			
$I_{OL}$	Output LOW Current	2.1			5.6						mA	MIN, 25°C MAX	$V_{OUT} = 0.4 \text{ V}$ for $V_{DD} = 4.5 \text{ V}$ Inputs at 0 V or $V_{DD}$ per Function
		3.3											
$I_{DD}$	Quiescent Power Supply Current			1			2			4	$\mu\text{A}$	MIN, 25°C MAX	All Inputs at 0 V or $V_{DD}$
				30			60			120			

Notes on the following page.

**GS CMOS · GD4049B · GD4050B**

**DC CHARACTERISTICS:**  $V_{DD}$  as shown,  $V_{SS} = 0\text{ V}$ , 4049BXC and 4050BXC (Cont'd) (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS
		$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			$V_{DD} = 15\text{ V}$					
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
$I_{OH}$	Output HIGH Current	-1.5									mA	MIN	$V_{OUT} = 2.5\text{ V}$ for $V_{DD} = 5\text{ V}$ Inputs at 0 or $V_{DD}$ per Function
		-1.25	-2.5										
		-1.0									mA	MAX	
		-0.6			-1.5			-4.5			mA	MIN	$V_{OUT} = 4.5\text{ V}$ for $V_{DD} = 5\text{ V}$ $V_{OUT} = 9.5\text{ V}$ for $V_{DD} = 10\text{ V}$ $V_{OUT} = 13.5\text{ V}$ for $V_{DD} = 15\text{ V}$ Inputs at 0 or $V_{DD}$ per Function
		-0.5	-1		-1.25	-2.5		-3.75	-7.5				
		-0.4			-1.0			-3			mA	MAX	
$I_{OL}$	Output LOW Current	3.6			9.6			28			mA	MIN	$V_{OUT} = 0.4\text{ V}$ for $V_{DD} = 5\text{ V}$ $V_{OUT} = 0.5\text{ V}$ for $V_{DD} = 10\text{ V}$ $V_{OUT} = 1.5\text{ V}$ for $V_{DD} = 15\text{ V}$ Inputs at 0 or $V_{DD}$ per Function
		3.0	6		8	16		24	48	mA			
		2.5			6.6			19				mA	MAX
		3.1									mA	MIN	$V_{OUT} = 0.4\text{ V}$ for $V_{DD} = 4.5\text{ V}$ Inputs at 0 V or $V_{DD}$ per Function
		2.6	5.2										
		2.1									mA	MAX	
$I_{DD}$	Quiescent Power Supply Current			4			8			16	$\mu\text{A}$	MIN, 25°C	All inputs at 0 V or $V_{DD}$
				30			60			120			

**AC CHARACTERISTICS AND SET-UP REQUIREMENTS:**  $V_{DD}$  as shown,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , 4049B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			$V_{DD} = 15\text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay		65	130		30	65		29	52	ns	$C_L = 50\text{ pF}$ , $R_L = 200\text{ k}\Omega$
$t_{PHL}$			50	105		25	50		17	40		
$t_{TLH}$	Output Transition Time		73	145		40	80		30	60	ns	Input Transition Times $\leq 20\text{ ns}$
$t_{THL}$			33	65		13	25		9	20		

**NOTES:**

- Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
- Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

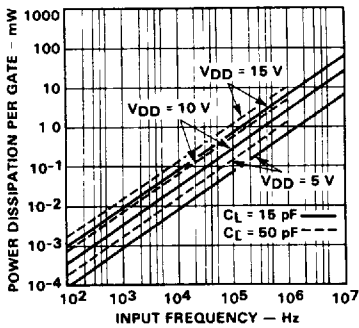
AC CHARACTERISTICS AND SET-UP REQUIREMENTS:  $V_{DD}$  as shown,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , 4050B only (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5\text{ V}$			$V_{DD} = 10\text{ V}$			$V_{DD} = 15\text{ V}$				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$ $t_{PHL}$	Propagation Delay		65	130		30	65		24	52	ns	$C_L = 50\text{ pF}$ , $R_L = 200\text{ k}\Omega$ Input Transition Times $\leq 20\text{ ns}$
$t_{TLH}$ $t_{THL}$	Output Transition Time		73	145		90	80		30	60		
			33	65		13	25		9	20		

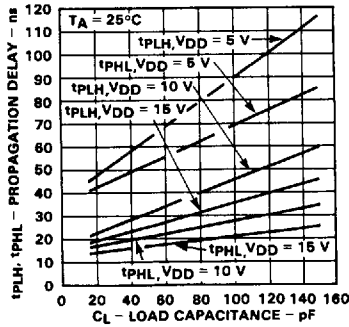
Notes on preceding page.

TYPICAL ELECTRICAL CHARACTERISTICS

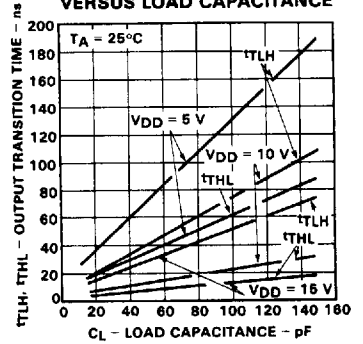
TYPICAL POWER DISSIPATION VERSUS FREQUENCY



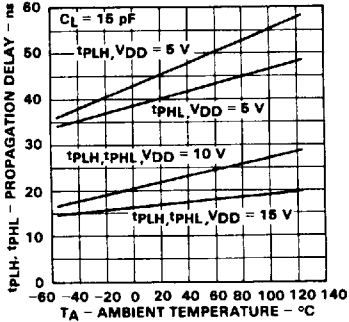
PROPAGATION DELAY VERSUS LOAD CAPACITANCE



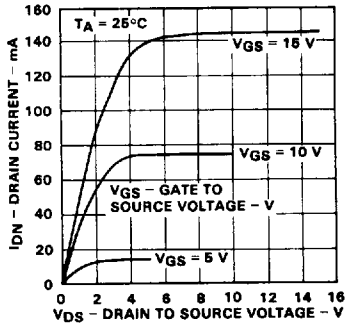
OUTPUT TRANSITION TIME VERSUS LOAD CAPACITANCE



PROPAGATION DELAY VERSUS TEMPERATURE



N-CHANNEL DRAIN CHARACTERISTICS



P-CHANNEL DRAIN CHARACTERISTICS

