Power Field Effect Transistor

N-Channel Enhancement-Mode Silicon Gate

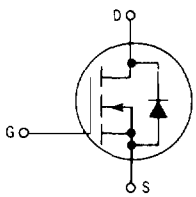
BUZ330

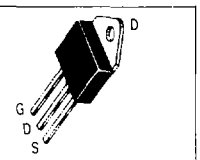
This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.6 Ω Max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™

TMOS POWER FET
9.5 AMPERES
$r_{DS(on)}$ = 0.6 OHMS
500 VOLTS





CASE 340-02
TO-218

3

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	500	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	500	Vdc
Gate-Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	9.5 38	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 500 Volts, V_{GS} = 0) (V_{DS} = 500 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 1.0 10	 80 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

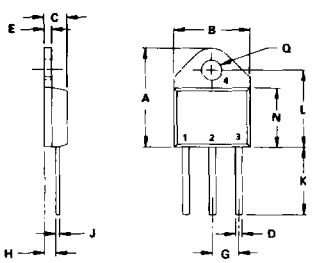
(continued)

ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 10 mA)		$V_{GS(th)}$	2.1	3.0	4.0	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$r_{DS(on)}$	—	0.47	0.6	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 9.5 Adc)		$V_{DS(on)}$	—	4.75	—	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 6.0 A)		g_{FS}	5.0	8.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	—	1800	pF
Output Capacitance		C_{oss}	—	—	270	
Reverse Transfer Capacitance		C_{rss}	—	—	120	
Total Gate Charge	(V_{DS} = 400 V, V_{GS} = 10 Vdc, I_D = 12.8 A)	Q_g	—	70	—	nC
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 2.8 A, V_{GS} = 10 V, R_{gen} = 50 ohms)	$t_{d(on)}$	—	—	40	ns
Rise Time		t_r	—	—	70	
Turn-Off Delay Time		$t_{d(off)}$	—	—	310	
Fall Time		t_f	—	—	90	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 19 A, V_{GS} = 0)	V_{SD}	—	1.0	1.4	Vdc
Forward Turn-On Time	(I_S = 9.5 A, dI_S/dt = 100 A/μs, V_R = 100 V)	t_{on}	Negligible			ns
Reverse Recovery Time		t_{rr}	—	400	—	

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

CASE 340-02
TO-218



STYLE 2
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.32	21.08	0.800	0.830
B	15.49	15.90	0.610	0.626
C	4.19	5.08	0.165	0.200
D	1.02	1.65	0.040	0.065
E	1.35	1.65	0.053	0.065
G	5.21	5.72	0.205	0.225
H	2.65	2.94	0.104	0.116
J	0.51	0.71	0.020	0.028
K	12.70	15.49	0.500	0.610
L	15.88	16.51	0.625	0.650
N	12.19	12.70	0.480	0.500
Q	4.04	4.22	0.159	0.166

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. Output Characteristics

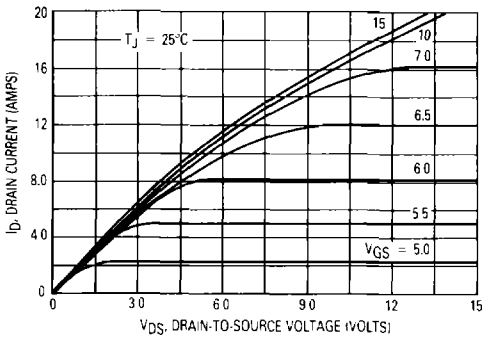


Figure 2. Gate-To-Source Threshold Voltage Variation With Temperature

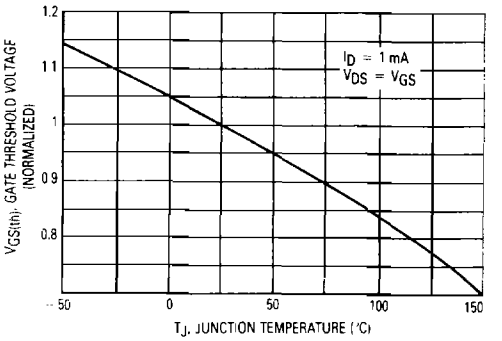


Figure 3. Transfer Characteristics

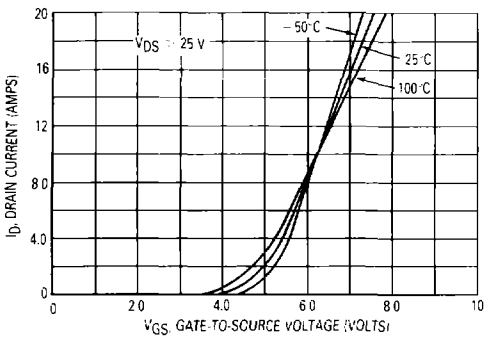


Figure 4. Breakdown Voltage Variation With Temperature

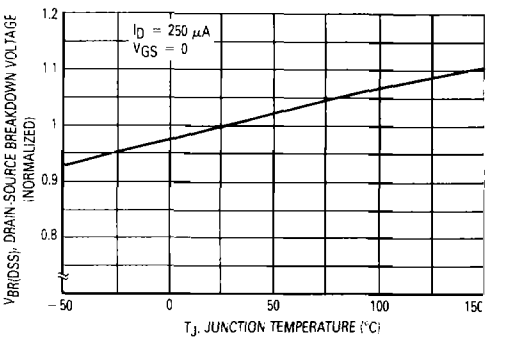


Figure 5. On-Resistance versus Drain Current

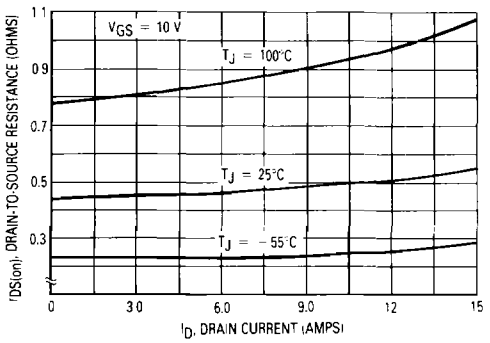
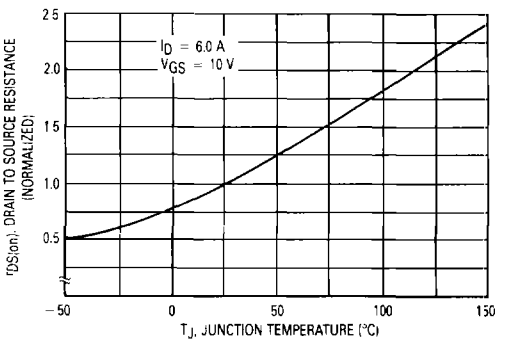


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

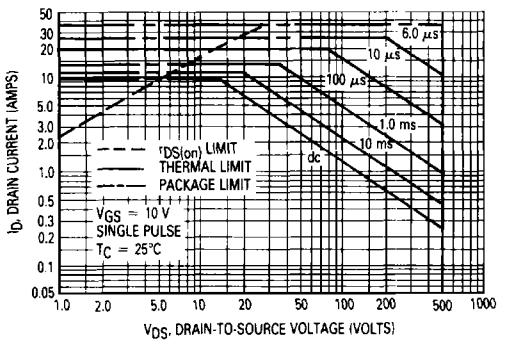
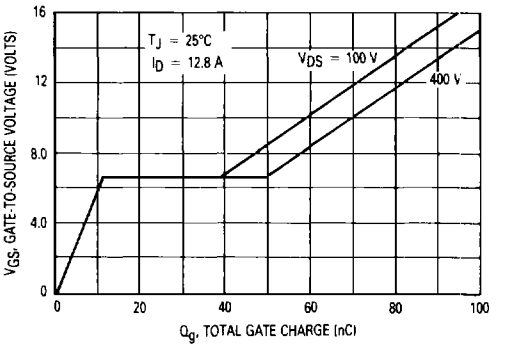


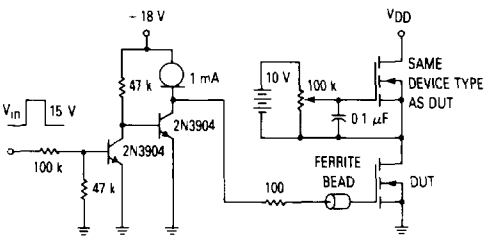
Figure 8. Gate Charge versus Gate-To-Source Voltage



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

Figure 9. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

Figure 10. Thermal Response