MAINTENANCE TYPE

BLX97

U.H.F. LINEAR POWER TRANSISTOR

N-P-N multi-emitter silicon planar epitaxial transistor primarily for use in linear u.h.f. amplifiers for television transposers and transmitters.

Features:
- guaranteed low intermodulation figures;
- gold metallization ensures excellent reliability.

The transistor has a ¼" capstan envelope with a moulded cap. All leads are isolated from the stud.

QUICK REFERENCE DATA

R.F. performance in linear amplifier

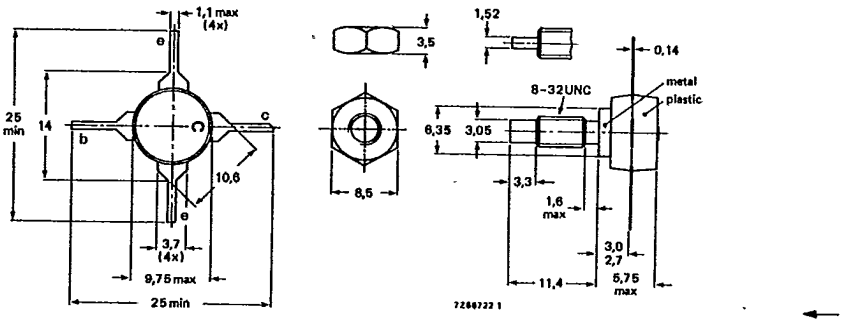
mode of operation	f_{vision} MHz	V_{CE} V	I_C mA	T_h °C	d_{im}* dB	$P_{o\ sync}$* W	G_p dB
class-A	860	25	500	25	−60	> 1,0	> 5,5
class-A	860	25	500	25	−60	typ. 1,1	typ. 6,5

* Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-48/3.



Torque on nut: min. 0,75 Nm (7,5 kg cm)
max. 0,85 Nm (8,5 kg cm)

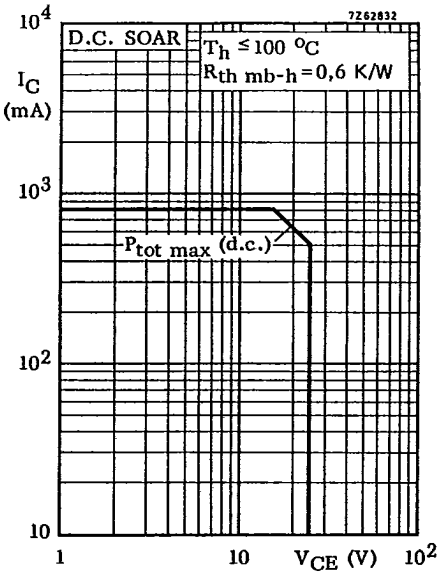
Diameter of clearance hole in heatsink: max. 4,2 mm.
Mounting hole to have no burrs at either end.
De-burring must leave surface flat; do not chamfer or countersink either end of hole.

When locking is required an adhesive is preferred instead of a lock washer.

PRODUCT SAFETY This device incorporates beryllium oxide, the dust of which is toxic. The device is entirely safe provided that the BeO disc is not damaged.

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC134)

Collector-base voltage (open emitter; peak value)	V_{CBOM}	max.	40	V
Collector-emitter voltage (R_{BE} = 10 Ω; peak value)	V_{CERM}	max.	40	V
Collector-emitter voltage (open base)	V_{CEO}	max.	27	V
Emitter-base voltage (open collector)	V_{EBO}	max.	3,5	V
Collector current (d.c.)	I_C	max.	0,8	A
Collector current (peak value) f > 1 MHz	I_{CM}	max.	2	A
Total power dissipation up to T_h = 100 °C	P_{tot}	max.	12,5	W



Storage temperature	T_{stg}	−65 to +200		°C
Junction temperature	T_j	max.	200	°C

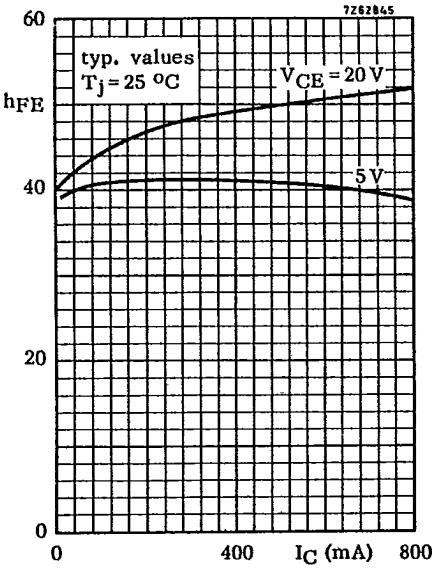
THERMAL RESISTANCE

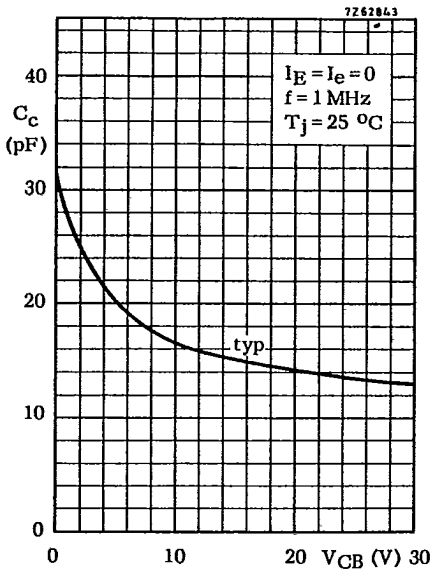
From junction to mounting base	$R_{th\ j\text{-}mb}$	=	7,5	K/W
From mounting base to heatsink	$R_{th\ mb\text{-}h}$	=	0,6	K/W

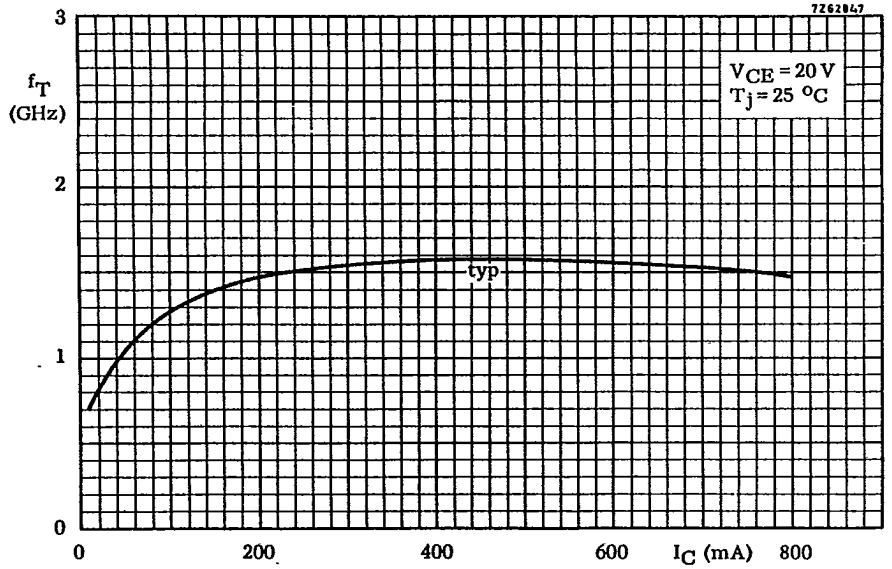
CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector cut-off current				
I_E = 0; V_{CB} = 20 V	I_{CBO}	<	200	μA
Breakdown voltages				
Collector-base voltage				
open emitter; I_C = 2 mA	$V_{(BR)CBO}$	>	40	V
Collector-emitter voltage				
R_{BE} = 10 Ω; I_C = 10 mA	$V_{(BR)CER}$	>	40	V
open base; I_C = 10 mA	$V_{(BR)CEO}$	>	27	V
Emitter-base voltage				
open collector; I_E = 2 mA	$V_{(BR)EBO}$	>	3,5	V
Saturation voltage				
I_C = 400 mA; I_B = 40 mA	V_{CEsat}	<	0,75	V
D.C. current gain				
I_C = 400 mA; V_{CE} = 20 V	h_{FE}	>	30	
I_C = 800 mA; V_{CE} = 20 V	h_{FE}	>	20	
Transition frequency				
I_C = 400 mA; V_{CE} = 20 V	f_T	>	1,2	GHz
I_C = 700 mA; V_{CE} = 20 V	f_T	>	1,0	GHz
Collector capacitance at f = 1 MHz				
$I_E = I_e$ = 0; V_{CB} = 20 V	C_c	<	20	pF
Feedback capacitance at f = 1 MHz				
I_C = 20 mA; V_{CE} = 20 V; T_{mb} = 25 °C	C_{re}	typ.	7	pF
Collector-stud capacitance	C_{cs}	typ.	2	pF





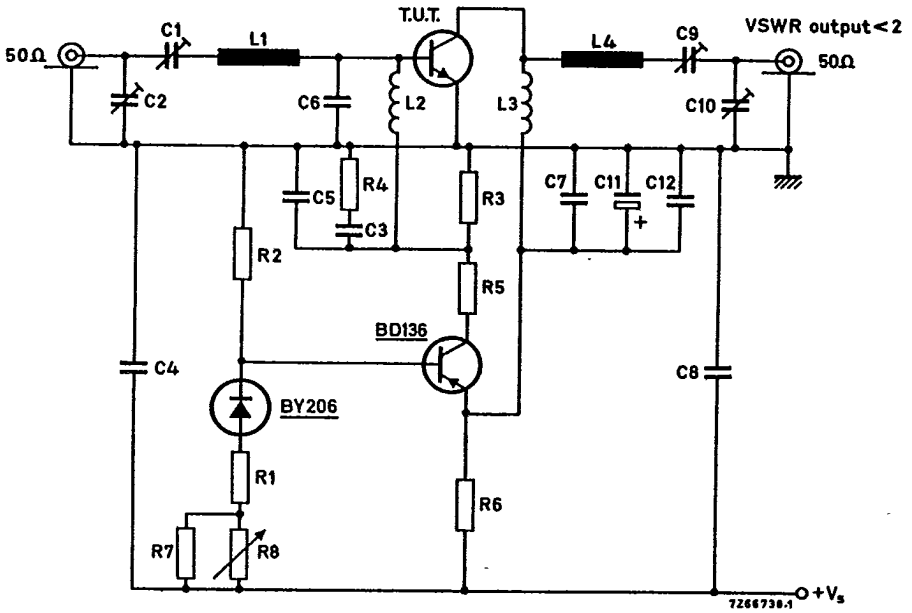


APPLICATION INFORMATION

d_{im} (dB) *)	f_{vision} (MHz)	V_{CE} (V)	I_C (mA)	G_p (dB)	$P_{o\ sync}$ (W) *)	T_h (°C)
−60	860	25	500	> 5,5	> 1,0	25
−60	860	25	500	typ. 6,5	typ. 1,1	25

*) Three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.

Test circuit at f_{vision} = 860 MHz



List of components: (see also page 6)

C1 = C2 = C10 = 2 to 9 pF film dielectric trimmers
C3 = C4 = C12 = 100 nF polyester capacitors
C5 = C7 = C8 = 100 pF feed-through capacitors
C6 = 2 x 2,7 pF in parallel, chip capacitors
C9 = 2 to 18 pF film dielectric trimmer
C11 = 10 µF/40 V solid aluminium electrolytic capacitor

R1 = 220 Ω
R2 = 4,7 kΩ
R3 = 100 Ω
R4 = 10 Ω
R5 = 470 Ω (1 W)
R6 = 3 x 22 Ω in parallel; (1 W)
R7 = 12 kΩ
R8 = 1 kΩ

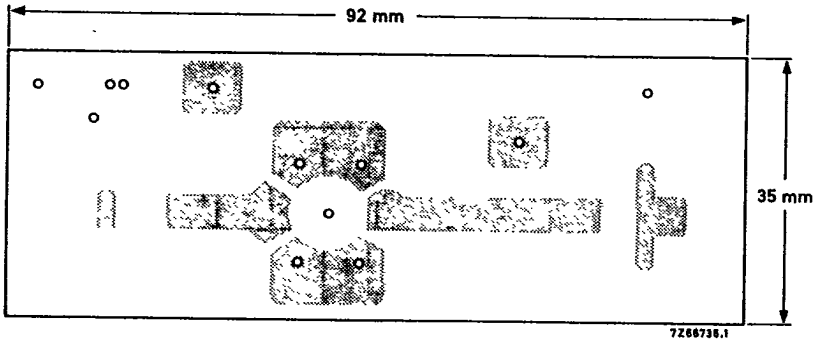
APPLICATION INFORMATION (continued)

List of components: (continued)

L1 = stripline (14,8 mm x 4,3 mm)
L2 = 7 turns closely wound enamelled Cu wire (0,5 mm); int. dia. 3 mm
L3 = 2 turns Cu wire (1 mm); winding pitch 1,5 mm; int. dia. 4,5 mm; leads 2 x 5 mm
L4 = stripline (29,5 mm x 4,3 mm)

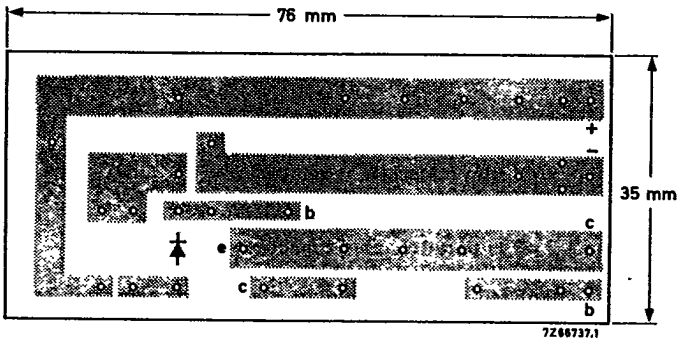
L1 and L4 are striplines on a double Cu-clad print plate with PTFE fibre-glass dielectric ($\epsilon_r = 2,74$); thickness 1,45 mm.

Layout of printed-circuit board for 860 MHz test circuit.



The circuit and the components are situated on one side of the PTFE fibre-glass board, the other side being fully metallized to serve as earth. Earth connections are made by means of hollow rivets.

Layout of printed board bias circuit.



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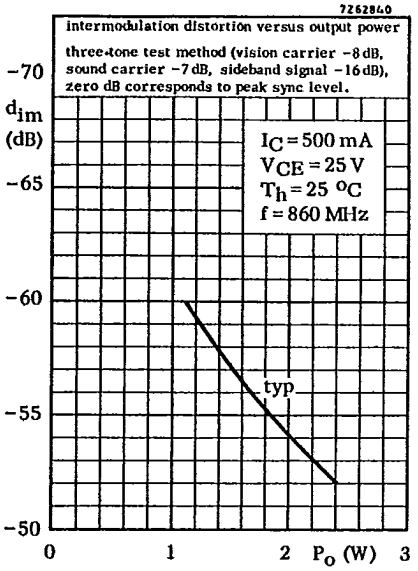
intermodulation distortion versus output power

three-tone test method (vision carrier −8 dB, sound carrier −7 dB, sideband signal −16 dB), zero dB corresponds to peak sync level.



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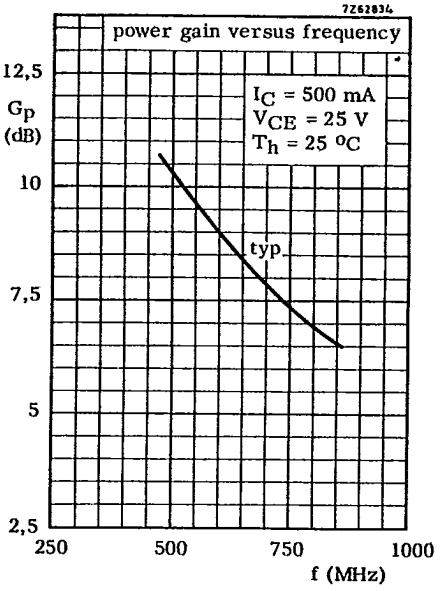
power gain versus frequency



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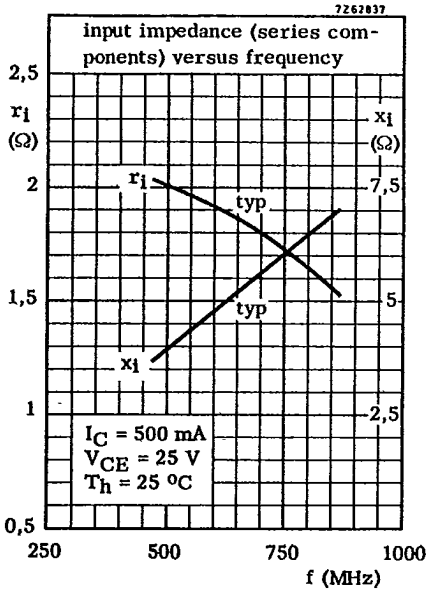
input impedance (series components) versus frequency



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load impedance (parallel components) versus frequency