INTERSIL

2N6483-2N6485
Low Noise Dual Monolithic N-Channel JFET

FEATURES

- Ultra Low Noise
  $\bar{e}_n < 10\ nV/\sqrt{Hz}$ at 10 Hz
- High CMRR > 100 dB
- Low Offset
  $\Delta\ |\ V_{GS1} - V_{GS2}\ | < 5\ mV$
- Tight Tracking
  $\Delta\ |\ V_{GS1} - V_{GS2}\ | / \Delta T < 5\ \mu V/°C$

ABSOLUTE MAXIMUM RATINGS (Note 1)
(@ 25°C unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ 85°C Free Air Temperature

One Side	250 mW
Both Sides	500 mW

Linear Derating

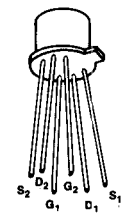
One Side	3.85 mW/°C
Both Sides	7.7 mW/°C

Maximum Voltages & Currents

V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
$V_{G1\,G2}$ Gate to Gate Voltage	±50 V
I_G Gate Current	50 mA

PIN CONFIGURATION

TO-71



CHIP TOPOGRAPHY

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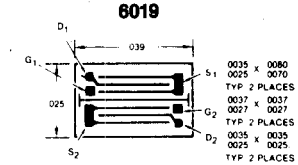


ORDERING INFORMATION

TO-71	WAFER	DICE
2N6483	2N6483/W	2N6483/D
2N6484	2N6484/W	2N6484/D
2N6485	2N6485/W	2N6485/D

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		200	pA	$V_{GS} = -30\ V, V_{DS} = 0, T_A = +25\ C$
			200	nA	$V_{GS} = -30\ V, V_{DS} = 0, T_A = +150\ C$
BV_{GSS}	Gate Source Breakdown Voltage	50		V	$I_G = 1\ \mu A, V_{DS} = 0$
V_p	Gate Source Pinch Off Voltage	0.7	4.0	V	$V_{DS} = 20\ V, I_D = 1\ nA$
I_{DSS}	Drain Current at Zero Gate Voltage	0.5	7.5	mA	$V_{DS} = 20\ V, V_{GS} = 0$ (Note 2)
g_{fs}	Common Source Forward Transconductance	1000	4000	μmho	$V_{DS} = 20\ V, V_{GS} = 0, f = 1\ KHz$ (Note 2)
g_{oss}	Common Source Output Conductance		10	μmho	$V_{DS} = 20\ V, V_{GS} = 0, f = 1\ KHz$
C_{iss}	Common Source Input Capacitance		20	pF	$V_{DS} = 20\ V, V_{GS} = 0, f = 1\ MHz$
C_{rss}	Common Source Reverse Transfer Capacitance		3.5	pF	$V_{DS} = 20\ V, V_{GS} = 0, f = 1\ MHz$
I_G	Gate Current		100	pA	$V_{GD} = 20\ V, I_D = 200\ \mu A, T_A = +25\ C$
			100	nA	$V_{DG} = 20\ V, I_D = 200\ \mu A, T_A = +150\ C$
V_{GS}	Gate Source Voltage	0.2	3.8	V	$V_{DG} = 20\ V, I_D = 200\ \mu A$
g_{fs}	Common Source Forward Transconductance	500	1500	μmho	$V_{DG} = 20\ V, I_D = 200\ \mu A, f = 1\ KHz$ (Note 2)
g_{os}	Common Source Output Conductance		1	μmho	$V_{DG} = 20\ V, I_D = 200\ \mu A$
$\bar{e}_n$	Equivalent Input Noise Voltage		10	$nV/\sqrt{Hz}$	$V_{DS} = 20\ V, I_D = 200\ \mu A, f = 10\ Hz$
			5	$nV/\sqrt{Hz}$	$V_{DS} = 20\ V, I_D = 200\ \mu A, f = 1\ KHz$

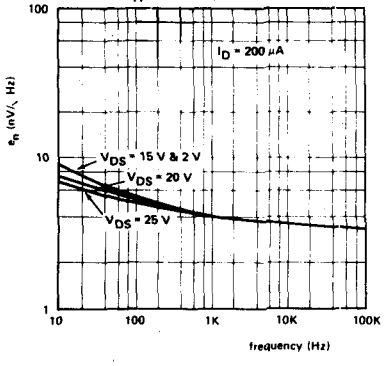
MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N6483		2N6484		2N6485		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125°C
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		0.1		0.1		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = +25°C to +125°C
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = -55°C to + 25°C
CMRR	Common Mode Rejection Ratio	100		100		90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

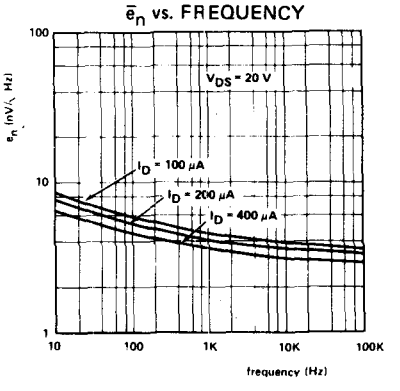
NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10 V), not included in JEDEC registration

TYPICAL OPERATING CHARACTERISTICS

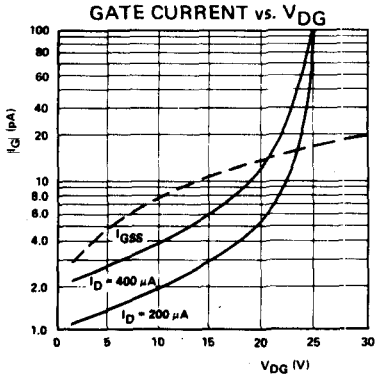
$\bar{e}_n$ vs. FREQUENCY



$\bar{e}_n$ vs. FREQUENCY



GATE CURRENT vs. V_{DG}



TYPICAL CAPACITANCE vs. V_{DS}